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Design and analysis of SOI and SELBOX junctionless FinFET at sub-15 nm technology node

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The structural and operational characteristics of a silicon on insulator (SOI) junctionless (JL) FinFET have been compared with the selective buried oxide (SELBOX) JL FinFET for 15 nm gate length and beyond using simulation studies. Simulations have been performed using silvaco TCAD (Atlas 3-D Module). SELBOX JL FinFET device has shown ~10 times improvement in I_{ON}/I_{OFF} ratio with respect to the SOI JL FinFET. The SELBOX based device has subthreshold slope (SS) value of 69.08 mV/Dec whereas this is 84.1 mV/Dec for SOI based device. SELBOX JL FinFET has DIBL value of 31.57 mV/V whereas this is 119 mV/V for SOI JL FinFET. The comparison results, discussed, are for the channel length (gate length) of 15 nm. Furthermore, short-channel characteristics for the n-channel and p-channel SELBOX JL FinFET have been discussed. For channel length of 5 nm (which is a future technology node for mass production of semiconductor devices and systems), SELBOX device has shown favourable value of I_{ON}/I_{OFF} ratio as 10^6 and SS as 96.86 mV/Dec. SELBOX JL FinFET has shown more immunity towards self-heating effect compared to the SOI JL FinFET. Performance of the SELBOX JL FinFET can be enhanced further independently by tuning various parameters such as the buried oxide thickness, the gap between buried oxide layers, substrate doping, and substrate bias.

Keywords: Junctionless transistor, Silicon on insulator (SOI) FinFET, Selective buried oxide (SELBOX) FinFET

1 Introduction

As the channel length of field effect transistors are reducing day by day, it's becoming really very tough to realize very sharp junctions. At very low channel length, a number of limitations such as Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Leakage (GIDL), I_{ON}/I_{OFF} ratio degradation etc. come into picture[1-2]. Few years back, a device with no junctions along the conduction path was proposed[3]. In this type of device, Source, Channel, and Drain, all have equal doping concentration. So, the problem of forming very sharp concentration gradient at junctions (Source-Channel and Channel-Drain) has been eliminated. Bulk FinFET, SOI FinFET, Multi-gate FinFET and gate-all-around junctionless nanowire (JNT) have been explored already[3-8]. Performance of SELBOX technology is also explored in[9-13] through 2-D/3-D simulations, where it has been established that SELBOX structures gives advantages in terms of self-heating effect over the SOI structure and also speed of operation is mid-way in between the SOI and BULK technology. This paper compares the performance of existing SOI Junctionless FinFET with the very recently proposed structure, *i.e.*, SELBOX Junctionless FinFET[14-15] at channel length 15 nm and beyond. SOI FinFETs have reasonably good On-state current and combat Short Channel Effects very well. However, the Multi-gate device based on SOI technology suffers from self-heating effect and also have low breakdown voltage[16]. In this work, we have compared the results of Junctionless FinFET structure based on Selective Buried Oxide (SELBOX) technology with the Multi-gate devices based on SOI technology at ultra-scaled gate length, i.e. up to 5 nm. Various parameters can be effectively controlled by varying the buried oxide thickness and spacing between buried oxides. This gap, given under the active region, connects the active and substrate region. It provides path for leakage current and hence for heat dissipation. So, problem of self-heating has been combated. The SELBOX device exhibits better I_{ON}/I_{OFF} ratio, DIBL, and SS with slight increase in threshold voltage, which in response has reduced the on-state current

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slightly. The SELBOX JL FinFET shows improved results even at 5 nm technology, which signifies that, it may be used in future technology node applications.

The paper has been presented in following sequence: In section 2, the simulation methods used and the parameters which have been considered for the device simulation are clearly expressed. In this section, the different performance parameters of the already existing device (SOI JL FinFET) and the very recently proposed device (SELBOX JL FinFET) have also been compared. At last, conclusion has been drawn in section 3.

2 Results and Discussion

Figure 1 presents the structure of simulated devices. All simulations are performed using Silvaco TCAD (Atlas 3-D Module)[17]. High-k dielectric material HfO_2 with dielectric constant value of 22 and effective oxide thickness of 1 nm and 15 nm of gate length are used for comparison. Simulation parameters for SOI JL FinFET have been taken as given in[18]. Gate work function for the SELBOX JL FinFET device is taken as 5 eV for n-type and 4.27 eV for p-type. Source, Channel and Drain concentrations, all are taken as 1.5 x 10^{19} cm^{-3} for both types of devices. Doping concentration of substrate in the n-type SELBOX device has taken as 5x10^{18} cm^{-3} of p-type. Values of all parameters taken for simulation are furnished in Table 1. The following models are included in the device simulation: ni.fermi, bqp.n, cvt, fldmob, consrh, auger, and bgn.

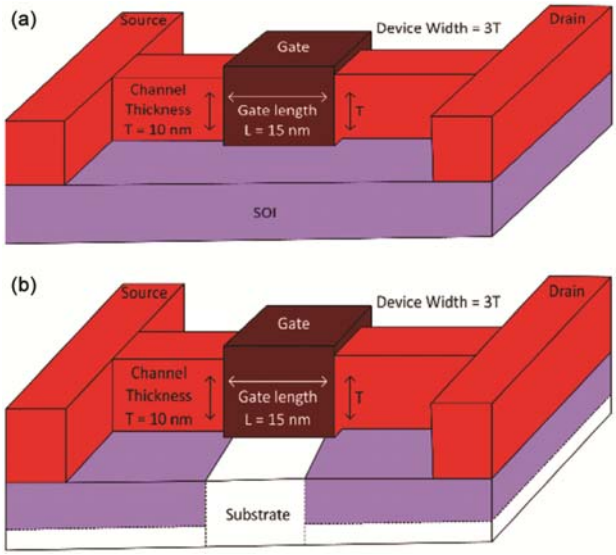

Fig. 1 — A 3D structural view of a (a) SOI JL FinFET and (b) SELBOX JL FinFET.

ni.fermi model combines the results of fermi statistics into the determination of the intrinsic concentration in formulae for SRH recombination. We have used Bohm Quantum Potential (bqp.n) correction model to include the effect of quantum mechanical confinement. cvt mobility model has been used to include parallel and perpendicular electric field effects, doping dependent, and temperature dependent effects. fldmob is used to model any type of effect which arises due to velocity saturation. consrh is used to depict SRH recombination using concentration dependant lifetimes. Auger model is used to probe auger recombination rate. Bandgap narrowing model is used to include bipolar current gain if present. The simulation model also includes band-to-band tunnelling model (bbt.hurks) and density gradient model (quantum3d) along with the above-mentioned models, especially for the calibrated graph. The quantization effects that arise because of very thin active layer have been taken into account. For the above-mentioned purpose, density-gradient model has been used. Band-to-band tunnelling model is used to take the concern of off-state band-to-band tunnelling leakage current. Figure 2 presents the calibration graph of reference[18]. Electron density distributions, under the gate for on-state of SOI JL FinFET and SELBOX JL FinFET, are shown in Fig. 3. For off-

Table 1 — Device parameters.

Parameters	**Value**	
	SOI JL FinFET	**SELBOX JL FinFET**
Fin height(H_{fin})/ Channel Thickness (T)	10 nm	10 nm
Buried oxide thickness	10 nm	10 nm
Fin width (T_{fin})	10 nm	10 nm
Channel length (L_G)	5-15 nm	5-15 nm
Thickness of substrate	80 nm	80 nm
Thickness of gate oxide (EOT)	1 nm	1 nm
Gate dielectric constant (ε_r)	22	22
Source, Channel, Drain doping	N: 1.5X10^{19} cm^{-3} P: 1.5X10^{19} cm^{-3}	N: 1.5X10^{19} cm^{-3} P: 1.5X10^{19} cm^{-3}
Substrate material	SiO_2	Silicon with N: 5X10^{18} cm^{-3}; P-type P: 5X10^{18} cm^{-3} ; N-type
Gate work function (Φ_M)	N: 5.0 eV P: 4.3 eV	N: 5.0 eV P: 4.27 eV
Gate oxide material	HfO_2	HfO_2

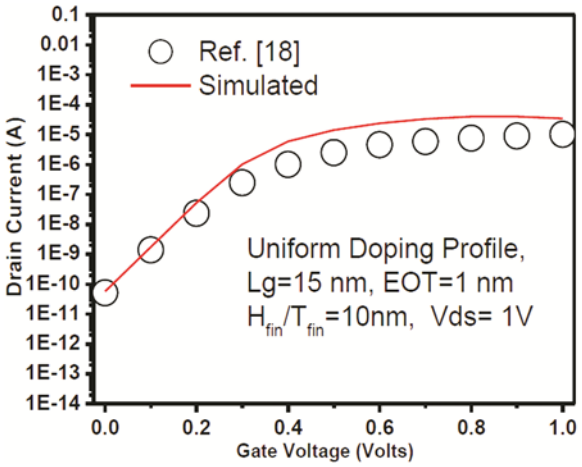

Fig. 2 — Calibrated graph of I_{DS}-V_{GS} characteristics of the BULK JL FinFET.

state, V_{GS} = 0 V and V_{DS} = 0.05 V has been taken. For on-state, V_{GS} = 1 V and V_{DS} = 0.05 V has been taken as defined in reference[18]. Electron density distribution under the gate for SELBOX device clearly shows that like other existing devices, the SELBOX FinFET also exhibits bulk conduction.

So, the SELBOX device will also not suffer from surface scattering. I_{DS}-V_{GS} curves for Junctionless SOI FinFET and SELBOX FinFET for gate length, L_G=15 nm, are shown in Fig. 4. From the graph, it is observed that the SELBOX device outperforms the existing ones. SELBOX JL FinFET device has better performance than the existing SOI JL FinFET and Junctionless Bulk FinFET[18] with respect to I_{ON}/I_{OFF} ratio by order of 10^1. DIBL of 31.57 mV/V is achieved for Junctionless SELBOX FinFET whereas

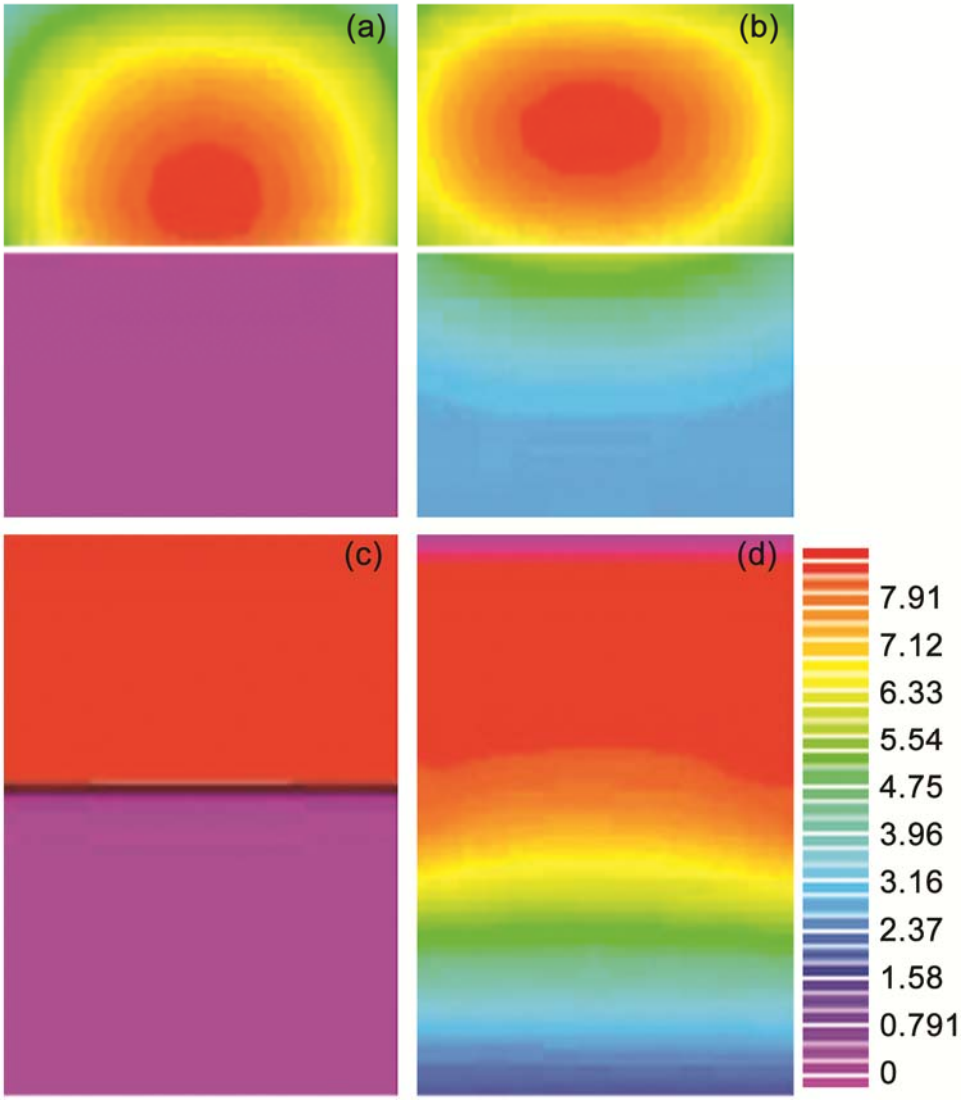

Fig. 3 — Off-state and on-state electron concentration distribution in the channel under gate.

this is 119 mV/V for Junctionless SOI FinFET and 40 mV/V for Junctionless Bulk FinFET[18] for the channel length of L_G = 15 nm. The SELBOX JL FinFET structure offers reduced DIBL even with respect to the Bulk JL FinFET[18]. The Junctionless SOI FinFET has SS = 84.1 mV/decade whereas the SELBOX device has SS = 69.08 mV/decade. At 15 nm gate length, Junctionless SOI FinFET has threshold voltage equal to 0.48 V whereas the SELBOX device has this value equal to 0.64 V. This is because of opening given under the gate in the SELBOX device. Junctionless SOI FinFET has slightly higher on-current value. I_{DS}-V_{GS} curves for n-channel and p-channel Junctionless SELBOX and SOI FinFET for different channel lengths are shown in Figs 5 and 6. From Fig. 6, it is observed that SOI FinFET has slightly higher on-current for all channel lengths. But, SOI FinFET has higher off-current for all considered channel lengths. This is because, depletion of carriers in the channel in SOI FinFET is not as effective as in SELBOX FinFET. Carriers deplete from both sides in the SELBOX FinFET i.e. from the upper as well as from the lower side of the channel. Subthreshold slope of SELBOX device is the best among all devices (including Bulk device) and its value is getting increased with decreasing channel length as shown in Figs 7 and 8. Variation of I_{ON}/I_{OFF} ratio with different channel length for the new device has also shown in Figs 7 and 8. From Figs 7 and 8, it is clearly seen that the on-off current ratio decreases with decreasing channel length, which is obvious due to short channel effects. By comparing the results shown in Figs 7 and 8, it can be observed and analysed that I_{ON}/I_{OFF} current ratio is pretty better in SELBOX FinFET. So, it will perform better in switching applications. SOI FinFET also has decreasing I_{ON}/I_{OFF} ratio with diminishing channel length just as in SELBOX FinFET due to short channel effects. But, unlike SOI FinFET, SELBOX FinFET has pretty good value of I_{ON}/I_{OFF} ratio even at the channel length of 5 nm. Change in threshold voltage with change in channel length for the SELBOX and SOI devices are shown in Figs 9 and 10. DIBL effect for different channel lengths, has also been simulated and results are presented in Figs 9 and 10. SELBOX device of p-type and n-type have different values of threshold voltage and hence different values of DIBL at all channel lengths. Threshold voltage decreases with decrease in channel length for both the devices, this is due to the fact that

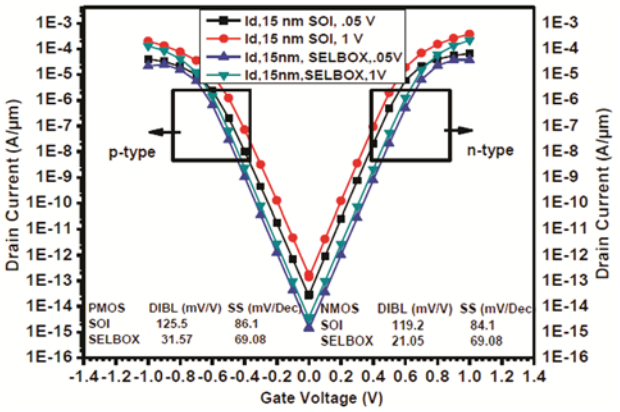

Fig. 4 — I_{DS}-V_{GS} curves of n-channel and p-channel junctionless SOI and SELBOX FinFETs with gate length, L_G = 15 nm, Fin height/width (H_{fin}/T_{fin}) = 10 nm, and EOT = 1nm.

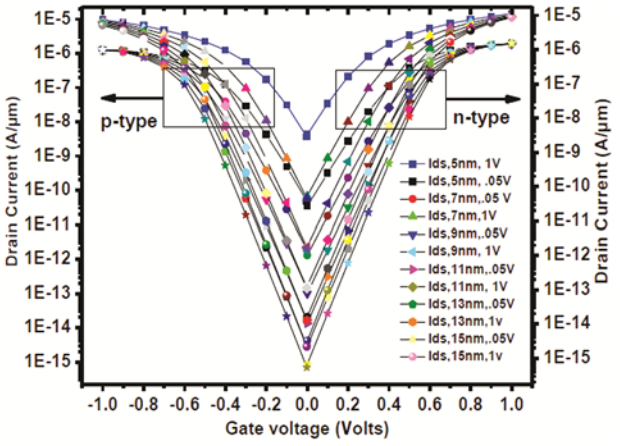

Fig. 5 — I_{DS}-V_{GS} curves of n-channel and p-channel junctionless SELBOX FinFET with different gate lengths.

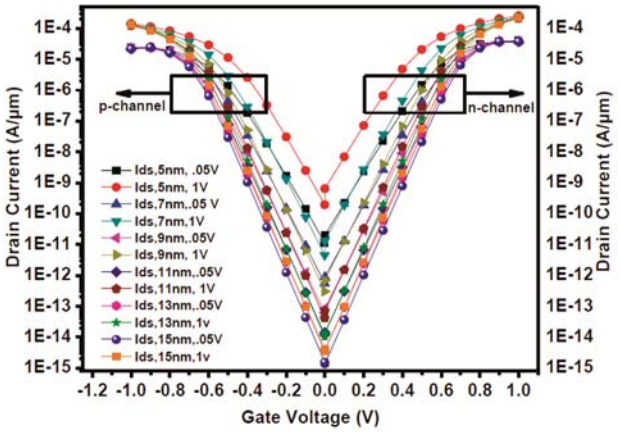

Fig. 6 — I_{DS}-V_{GS} curves of n-channel and p- channel junctionless SOI FinFET with different gate lengths.

gate losses control at smaller channel lengths due to short channel effects. For channel length of 5 nm, the SELBOX device shows favourable value of I_{ON}/I_{OFF}

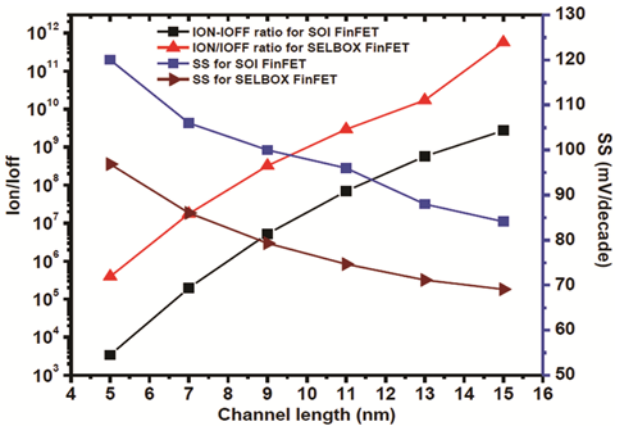

Fig. 7 — I_{ON}/I_{OFF} ratio and subthreshold slope variation versus different channel lengths for n-channel Junctionless SOI and SELBOX FinFET.

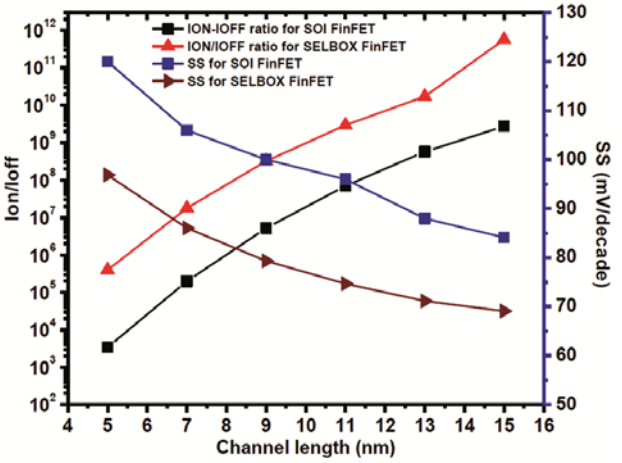

Fig. 8 — I_{ON}/I_{OFF} ratio and subthreshold slope variation versus different channel lengths for p-channel junctionless SOI and SELBOX FinFET.

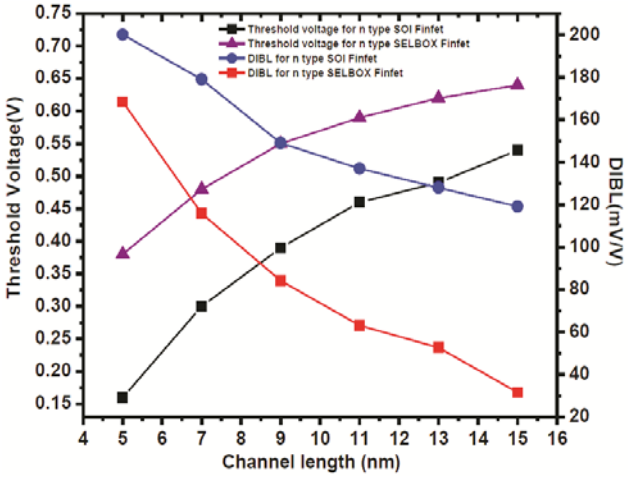

Fig. 9 — Threshold voltage and DIBL variation versus different channel lengths for n-channel Junctionless SOI and SELBOX FinFET.

ratio as ~10^6 and SS value as 96.86 mV/Dec. DIBL value of SOI FinFET has greater value than DIBL of SELBOX FinFET at each channel length which are shown in Figs 9 and 10. It is observed from Fig. 10 that there is small drop in on-current for SELBOX FinFET as compared to SOI FinFET. But, off-current of SELBOX FinFET is lower and vary faster than SOI FinFET at each channel length. Figures 11 & 12 show the variation of on and off current of SOI and SELBOX FinFET with varying channel length.

Very small drop in on-current of SELBOX FinFET is due to the opening given under the gate which lowers the electric field strength between source and drain. off-current of SELBOX FinFET is lower due to depletion of carriers from both sides i.e. from the top as well as from the bottom of the channel. Threshold voltage has been calculated by constant current method and DIBL has been calculated by the formula given in reference[9]. In SELBOX FinFET, opening

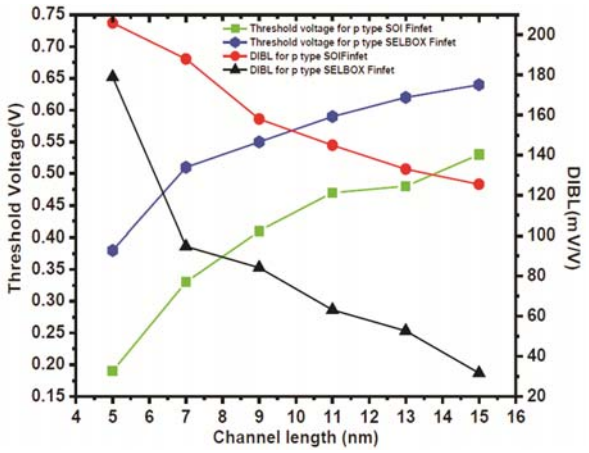

Fig. 10 — Threshold voltage and DIBL variation versus different channel lengths for p-channel Junctionless SOI and SELBOX FinFET .

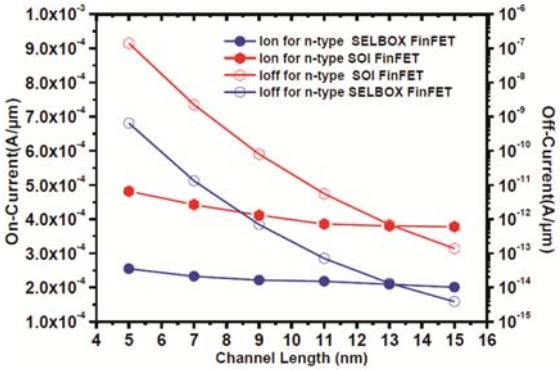

Fig. 11— I_{ON} and I_{OFF} variation versus different channel lengths for n-channel Junctionless SOI and SELBOX FinFET.

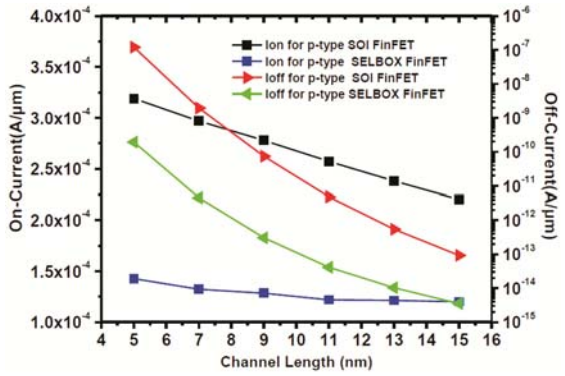

Fig. 12 — I_{ON} and I_{OFF} variation versus different channel lengths for p-channel Junctionless SOI and SELBOX FinFET.

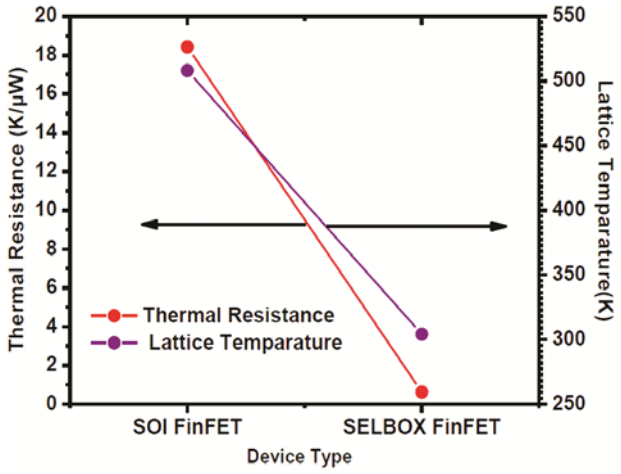

Fig. 13 — Thermal resistance and lattice temperature of junctionless SOI and SELBOX FinFET at V_{DS}=1V, V_{GS}=1V, and L_G=15 nm. L_{SELBOX} =15 nm.

given under the gate provides path for leakage current and so this reduces heating of the device. Immunity against self-heating of the device can be determined and compared with the help of measurement of the parameter, thermal resistance. Thermal resistance depends on the power dissipation and lattice temperature of the device. The expression used to determine thermal resistance is taken as mentioned in reference[17-18]. The device having larger value of thermal resistance, will have lesser immunity against self-heating. It has been shown and well established that SELBOX FinFET has lower value of thermal resistance than SOI FinFET at equal channel lengths[14]. Lat.temp model is included in the simulation to determine lattice temperature at V_{DS}=1V, V_{GS}=1V, and L_G=15 nm for both devices. For SELBOX FinFET, L_{SELBOX} =15 nm is used. The graph of lattice temperature and thermal resistance for SELBOX and SOI FinFET is shown in Figure 13. SELBOX FinFET has lower value of thermal resistance and lattice temperature than SOI FinFET. So, SELBOX FinFET shows more immunity against self-heating than SOI FinFET. SELBOX FinFET can be made more immune against self-heating by increasing the gap under the active layer. So, the new device can sustain on higher temperature than SOI FinFET. From Figure 7, 8, 9, 10, 11 and 12 we can see that SELBOX JL FinFET outperforms SOI JL FinFET at every channel length with respect to all performance parameters except for the values of on-current (speed of operation).

3 Conclusions

This paper has presented the design and electrical characteristics analysis of existing Junctionless SOI FinFET with the recently proposed Junctionless SELBOX FinFET at sub-15 nm channel length through 3D simulation studies. Simulation results show that the Junctionless SELBOX FinFET has higher I_{ON}/I_{OFF} current ratio, lower DIBL, lower subthreshold slope and better short channel behaviour even at ultra-short channel length, i.e., at 5 nm. Like the existing ones, the recently proposed device also undergoes bulk conduction. So, the new device is also free from surface scattering. Enhanced results of Junctionless SELBOX FinFET show that this device could be used in coming technology node application.

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