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Digitally controlled sigma-delta modulated direct matrix converter for high frequency AC-AC Conversion

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In recent times, several digitally controlled modulation techniques (MTs) have envisioned for generating pulse width modulation (PWM) trigger pulses to improve the quality of the output (o/p) produced [in terms of reduced total harmonic distortion (THD)], from direct matrix converter (DMC). The development of a digital controller for single-phase DMC, producing o/p frequencies higher than the input frequency has been dealt with in this paper. Performance of the proposed DMC has been analysed by applying an advanced modulation technique, named as "Sigma-Delta modulation". The complete system has been simulated on the MATLAB/SIMULINK platform as well as successfully implemented on the real-time digital simulator "OPAL-RT: OP4510". Working of the proposed digital controller has been successfully verified for the DMC with o/p frequency, ranging from 100 Hz to 60 kHz. With the Sigma-Delta modulated trigger pulses, the lowest THD (associated with o/p voltage of the DMC) is found to be around 3.1 %. As the real-time results have been acquired in the close vicinity and conformity to the results achieved with simulations, this validates success of the proposed digital controller.

Keywords: Direct matrix converter, Field programmable gate arrays, Modulation techniques, Pulse width modulation, Sigma-delta modulation, Total harmonic distortion

1 Introduction

Importance of renewable energy has depended on the perceived risks of using fossil fuels[1,2]. Due to increasing demand of the electricity, generation of renewable energy has been augmented to counterbalance the depletion of non-renewable energy sources[3]. Production of the electricity, from Renewable energy conversion systems (RECS), involves variety of power electronics converters (PECs). These PECs generally employ many switching devices, which must be properly triggered and controlled.

The development of digital controllers to produce pulse width modulation (PWM) pulses for PECs has been a point of keen interest in the academia, researchers and the fraternity from industrial electronics[4-6]. Several digital circuits (based on micro-processor/ controller) can be used to generate PWM pulses[7]. However, the performance of these processors is quite restricted, as these are based on generic hardware. Sole dependency on software, to create, the application specific functionalities, imposes a great limit to design engineers too[8,9].

In contrast, the Field programmable gate arrays (FPGA) based digital controllers can provide the freedom to form customizable functionalities, wholly adapted to special requirements, pertaining to specific application(s)[10-13]. The FPGA based design, enables easy customization of both the hardware as well as the software also, at a very nominal budget[14-16].

This paper is all about developing a digital controller, implemented on the real-time digital simulator "OPAL-RT: OP4510 (utilizing Kintex-7 FPGA)" to produce firing signals applied to a direct matrix converter (DMC)[17-22]. The proposed single-phase DMC can produce output (o/p) signals with frequencies higher than the input (i/p) frequency. The proposed DMC can be used for many applications, few are listed as follows:

a. Wind energy conversion systems[3],
b. As the main/ auxiliary high frequency isolated grid-connected converter for the Battery energy storage system (BESS)[22-24],
c. As a primary converter for the high frequency conversion applications, in the contact-less charging of the Electrical vehicles (EVs)[25,26] and may more similar applications.

Because of regular is witching of power switches, the produced o/p voltage comprises of a lot of harmonics. These harmonics are required to be

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minimized[12-14,26-28]. For minimizing the total harmonic distortion (THD), triggering signals sent to every power IGBT switch, can be modulated employing a range of modulation techniques (MTs)[9-16,27,28]. The most commonly used and the basic carrier-based MT is the Sinusoidal pulse width modulation (SPWM)[9,14]. In this paper, an advanced MT, Sigma-delta modulation (SDM) has been explained in detail and successfully implemented, to reduce the unwanted THD content associated with o/p voltage of the proposed DMC. The comparative performance analysis of the DMC has been carried out for the simulated as well as the real-time results, by considering the THD values associated with the o/p voltage with frequency values, ranging from 100 Hz to 60 kHz.

2 Power circuit of the direct matrix converter

The power circuit of proposed single-phase DMC is illustrated in Fig. 1. A single phase 220 volts, 50 Hz source is used as an i/p supply. The schematic employs four (4) bi-directional power switches, which can block the voltage and conduct the current in both the directions. Alternately, when bi-directional switches are not available, the Insulated gate bi-polar transistors (IGBTs) arranged in the Common emitter (CE) configuration, along with a pair of diodes, can also be employed, as illustrated in Fig. 2. The IGBT

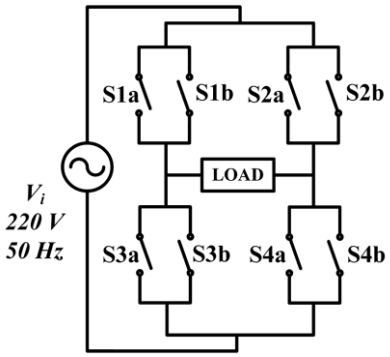

Fig. 1 — Power circuit of the proposed DMC.

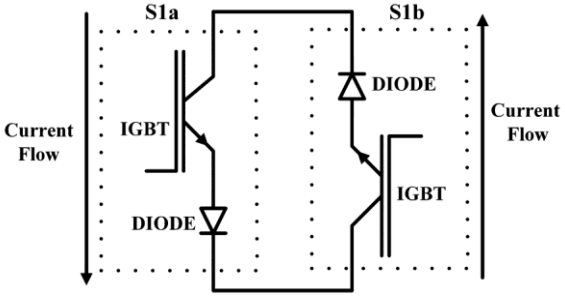

Fig. 2 — IGBT switches (Common emitter configuration).

power switches are preferred, as these possess comparatively higher switching capabilities as well as higher capacity for carrying the current[16]. These characteristics are quite desired for utilizing the proposed DMC to produce the o/p, for certain applications, requiring the higher power[14]. The expected o/p voltage can be produced from the DMC by appropriate triggering of the IGBT switches, ensuring the two (2) peculiar conditions. These conditions are:

The IGBTs should not short-circuit the voltage sources and the IGBTs should not open-circuit the current sources[27].

3 Principle of working

The single-phase DMC can produce o/p signals varying with a frequency, f_o generally related to the frequency of the i/p signal, f_i with a formula:

$$f_o = N.f_i \qquad \ldots(1)$$

where N is an integer.

By properly choosing switching sequence of the IGBT switches for a particular setting/ value of N, the o/p voltage for higher o/p frequencies (than f_i) can be produced. For example, when the value of f_o is set as double of the f_i, i.e. $f_o = 2.f_i$, the desired o/p voltage can be produced by employing the following switching sequence of the IGBT switches.

Case 1: When required o/p voltage is of positive polarity and i/p source voltage is also of the positive polarity, then the o/p waveform for this condition can be synthesized by triggering of the switches S1a and S4a.

Case 2: When required o/p voltage is of negative polarity and i/p source voltage is of positive polarity, then the o/p waveform for this condition can be synthesized by triggering of the switches S2a and S3a.

Case 3: When required o/p voltage is of positive polarity and i/p source voltage is of negative polarity, then the o/p waveform for this condition can be synthesized by triggering of the switches S3b and S2b.

Case 4: When required o/p voltage is of negative polarity and i/p source voltage is also of the negative polarity then the o/p waveform for this condition can be synthesized by triggering of switches S4b and S1b.

Therefore, to generate desired o/p signal of frequency double to that of the i/p frequency, the

adopted firing sequence is as shown in Fig. 3 (mentioned at the bottom side). Standard i/p and o/p waveforms for the DMC are also shown in Fig. 3.

4 Modulation technique

Because of regular switching of the power IGBTs, o/p voltage generated from the proposed single-phase DMC comprises of harmonics. The quality of the produced o/p voltage can be improved by reducing these harmonics. As the proposed DMC can generate o/p voltage with $f_o = N.f_i$, therefore the routine way of employing filter(s) is not very effective in this case for minimizing the THD content. This is because of the fact that, the generated o/p voltage can have different frequency values.

Alternately, for reducing these harmonics, the firing pulses applied to trigger the IGBT switches can be modulated. Therefore, the effective way to deal with the situation is to commission advanced MTs[9-16, 27,28]. Thorough description of the SDM used for the proposed DMC is stated in the following sections:

4.1 Delta modulation (DM)

The delta modulated signal can be produced by regularly tracking the modulating signal (MS), $e_m(t) = E_m sin(\omega_i t)$, applied as the reference or i/p signal to the delta modulator. The block diagram (BD) of a general DM system is shown in Fig. 4. It comprises of a closed-loop system incorporated with a hard limiter (or quantizer) in the forward path and an integrator (acting as a low pass filter) in the feed-back path[12]. The basic tasks, performed in the delta modulator are summarized as follows:

a. To produce samples of the MS, $e_m(t)$ periodically,
b. To compare the current value of the sample with that of the prior one and
c. Then to yield an o/p (modulated) signal of 1-bit.

The produced delta modulated signal, $e_{mod}(t)$ is of pulsating nature having variable width. The carrier signal, $e_c(t)$ is produced by carrying out the act of low pass filtering on the o/p signal, $e_{mod}(t)$. The standard waveforms of $e_m(t)$, $e_c(t)$ and $e_{mod}(t)$ are depicted in Fig. 5, for the DM System. For DM, the depth of modulation, m_d is given as:

$$m_d = \frac{E_m}{E_c}, \; for \; 0 < m_d < 1 \qquad \ldots(2)$$

4.2 Sigma-Delta modulation

For DM, the system comprises of a closed-loop, which confirms that the o/p of an integrator faithfully tracks the MS, $e_m(t)$. This implies that, whenever $e_m(t)$ increases in terms of frequency, it causes an increment in amplitude of the component of the modulated signal, $e_{mod}(t)$ at that frequency. Therefore, the amplitude transfer characteristic of the

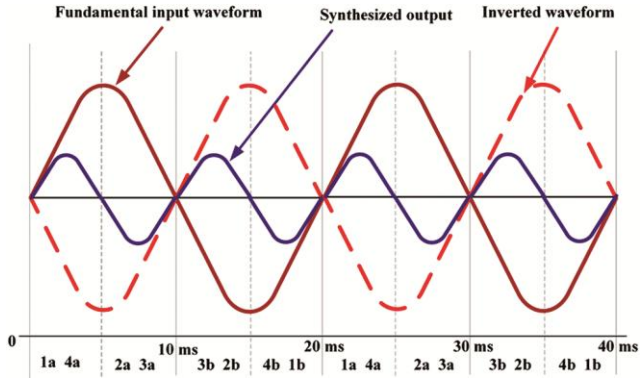

Fig. 3 — DMC waveforms along with firing patterns of the IGBTs for f_oi=i2f_i.

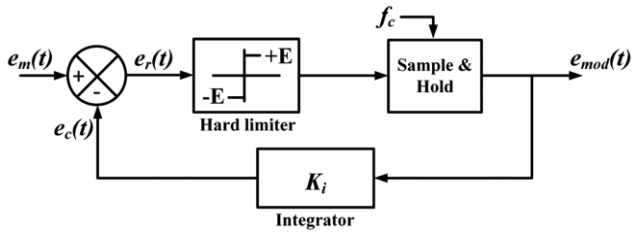

Fig. 4 — Block diagram of delta modulator.

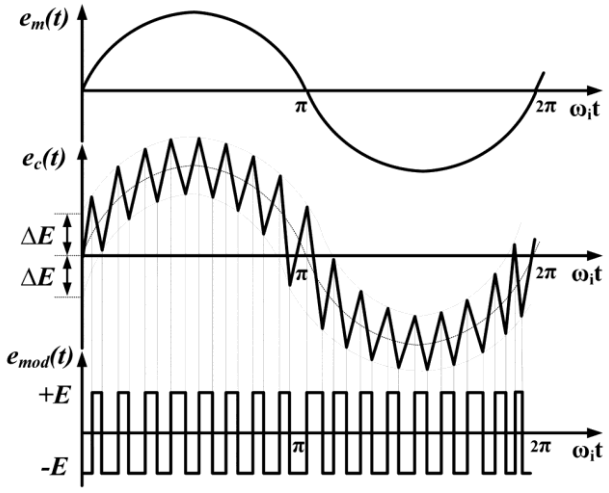

Fig. 5 — Delta modulation waveforms.

DM imitates very strong frequency dependence[16]. From the basic explanation of the DM system, it can be observed that, in order to ensure the faithful tracking of $e_m(t)$ by the CS $e_c(t)$, the condition for slope-overload (SO) must be avoided[27]. This necessitates an important condition that the derivative of $e_m(t)$ should always be less than or equal to the maximum rate of change of $e_c(t)$.

Suppose,

$$e_m(t) = E_m \sin(\omega_i t) \quad \ldots (3)$$

$$\left|\frac{d[e_m(t)]}{dt}\right|_{\max} = \omega_i E_m \quad \ldots (4)$$

$$\left|\frac{d[e_c(t)]}{dt}\right|_{\max} = K_i E \quad \ldots (5)$$

where,

ω_i = Frequency of the MS, $e_m(t)$, in Rad/Sec,

E = Switching level of the modulated signal $e_{mod}(t)$,

K_i = Gain of the Integrator.

From equations (4) and (5), it can be observed that:

$$\omega_i E_m \le K_i E \quad \ldots (6)$$

From equation (6), it is noticeable that the DM system can only faithfully encode the high frequency MS $e_m(t)$, if the condition for the SO is avoided. This also imposes a restriction on the amplitude of $e_m(t)$. The inter-dependence of the frequency ω_i and amplitude E_m of $e_m(t)$, for the condition of the SO can be removed by performing the integration on $e_m(t)$ too and setting the K_i appropriately. These modification results in to a new and better performing MT, known as the SDM. Again for $e_c(t)$ to track $e_m(t)$, the slope (max) of $e_m(t)$ $\le$ slope (max) of $e_c(t)$. Therefore,

$$e_m(t) = K_i \int V_i \, dt = K_i \int E_m \sin(\omega_i t) dt \quad \ldots (7)$$

$$e_m(t) = -\frac{K_i}{\omega_i} E_m \cos(\omega_i t) \, dt \quad \ldots (8)$$

Hence, the condition for the SO would be:

$$E_m \le E \quad \ldots (9)$$

The SDM is an improved form of the DM, which can avoid the condition for the SO[28]. The BD of the SDM is illustrated in Fig. 6. It comprises of a closed-loop system incorporated with an integrator, a hard-limiter and a sample and hold (SH) block connected in the forward path and comprises the unity feedback path. By incorporating the integrator block in forward path and by utilizing the unity feedback, the condition for SO can be made independent of the frequency ω_i of $e_m(t)$.

Employing the integrator in forward path exhibits, significantly zero error (steady state) for every reference, having a frequency, which is far lesser than the frequency of sampling, f_c. The produced SDM signal, $e_{mod}(t)$ is a pulsed waveform with variable width. The integrator (incorporated in the forward path), produces an estimated signal waveform (carrier signal), $e_c(t)$ from the difference of $e_m(t)$ and $e_{mod}(t)$, by performing the action of low pass filtering. The $e_c(t)$, thus produced is forwarded to the quantizer block and then to SH block, thereby generating the vital SDM signal as the o/p. For SDM, the waveforms of $e_m(t)$, $e_c(t)$ and $e_{mod}(t)$ are shown in Figs 7(a), (b) and (c), respectively.

5 Simulated Results

The simulation studies are carried out for the proposed single-phase DMC using SIMULINK/ MATLAB platform, for different settings of the o/p frequency, f_0 extending from 100 Hz to 60 kHz. The load considered under tests, employs a resistance, R = 10 kΩ and inductance, L = 100 mH. With these parameters, the measured THD value is found to be

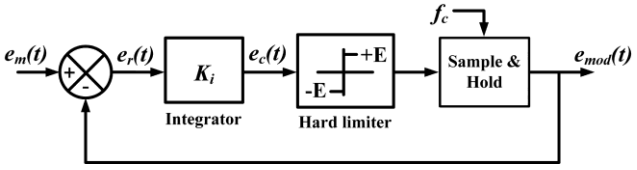

Fig. 6 — Block diagram of the sigma-delta modulator.

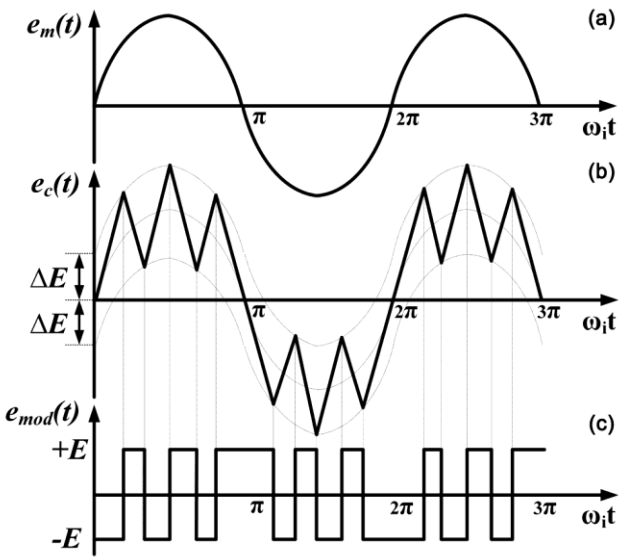

Fig. 7 — Waveforms of the sigma-delta modulator:
(a) Modulating signal, (b) Carrier signal and (c) Modulated signal.

the least for a setting of the 100 % depth of modulation, i.e. m_d = 1. For this reason, results from simulation studies are presented for the SDM technique, by setting the m_d = 1 and for the following two o/p frequency values:

a. f_o = 500 Hz (N = 10), showing waveforms of the o/p voltage and the THD allied with the o/p voltage, in Figs 8(a) and (b), respectively and

b. f_o = 5 kHz (N = 100), showing waveforms of the o/p voltage and the THD allied with the o/p voltage, in Fig. 9 (a) and (b), respectively.

From, the performance curves of DMC o/p voltage and the THD allied with o/p voltage, the observed THD appears to be 4.0 % and 3.4 %, as presented in Figs 8(b) and 9(b) for values of the f_o = 500 Hz and 5 kHz respectively. The comparative performance analysis through, simulation studies of the proposed

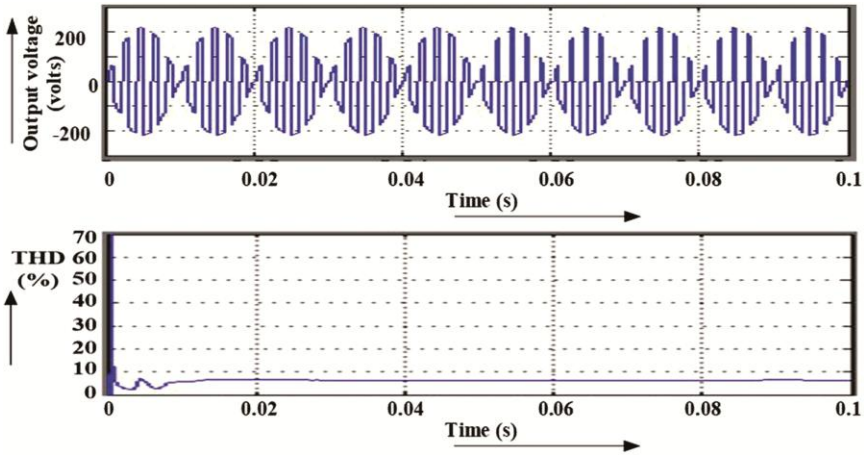

Fig. 8 — Performance curves of the DMC with SDM at f_o = 500 Hz:
(a) o/p voltage and (b) THD waveform associated with o/p voltage.

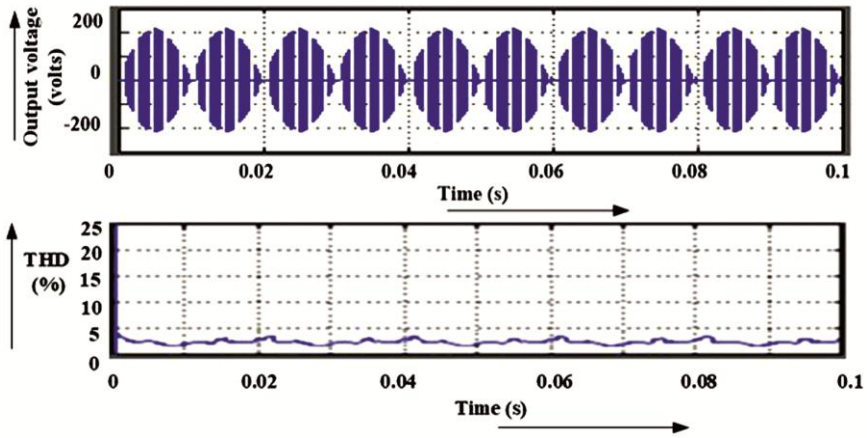

Fig. 9 — Performance curves of the DMC with SDM at f_o =i5ikHz:
(a) o/p voltage and (b) THD waveform associated with o/p voltage.

DMC with the SDM technique is illustrated in Fig. 10, with variations in f_0 .

6 Real-Time Results

Real-time results have been achieved on the real-time digital simulator "OPAL- RT: OP4510 (utilizing the Kintex-7 FPGA)" for the proposed DMC. These results have been captured for the different settings of f_0 with the SDM, by observing o/p waveforms on a mixed signal oscilloscope "Yokogawa: DLM2024".

Experimental setup of the real-time digital simulator is shown in Fig. 11. The OP4510 is a compact high-performance real-time digital simulator with faster processor up to 3.5 GHz. Architecture of the "OPAL-RT: OP4510" real-time digital simulator is shown in Fig. 12. Waveforms of the o/p voltage and the associated THD for the DMC have been captured for different settings of the f_0 with the SDM. These real-time results of the o/p voltage and the associated THD waveforms are shown for o/p frequencies, f_0 = 500 Hz and 5 kHz in Figs 13 and 14, respectively.

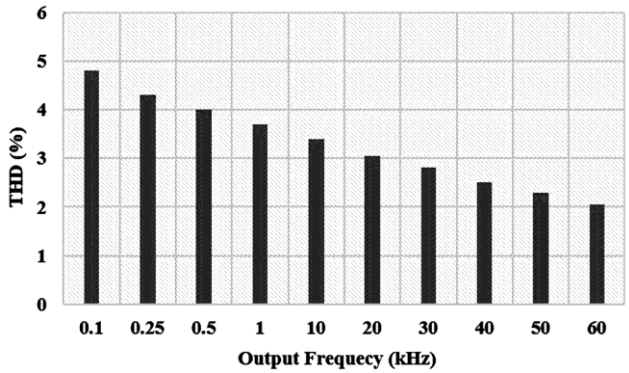

Fig. 10 — Software based performance analysis of the proposed DMC.

Fig. 11 — Setup of OPAL-RT: OP4510 real-time digital simulator.

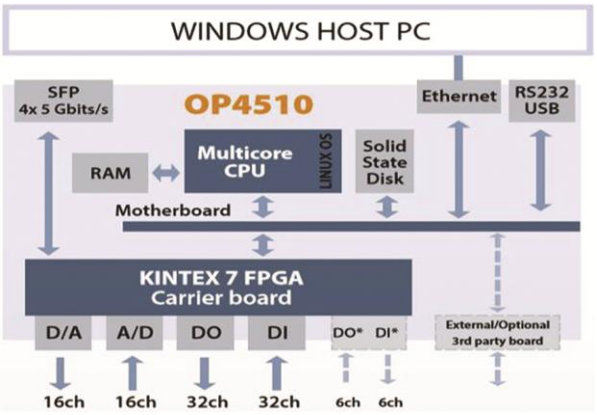

Fig. 12 — Architecture of the OPAL-RT's OP4510

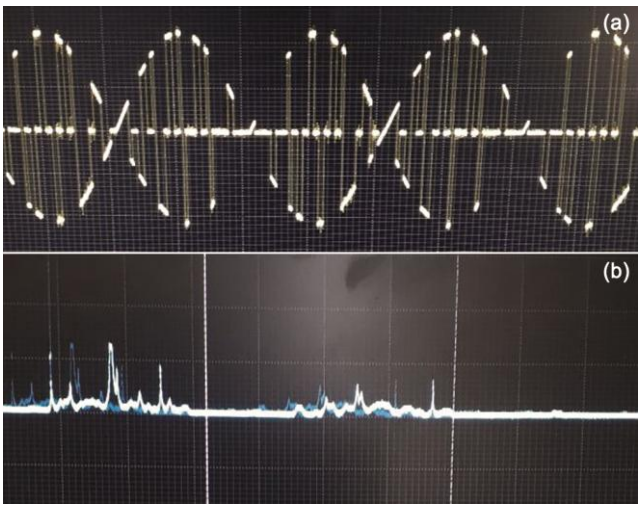

Fig. 13 — Real-time results of the DMC with SDM at f_o = 500 Hz: (a) o/p voltage and (b) THD waveform associated with o/p voltage.

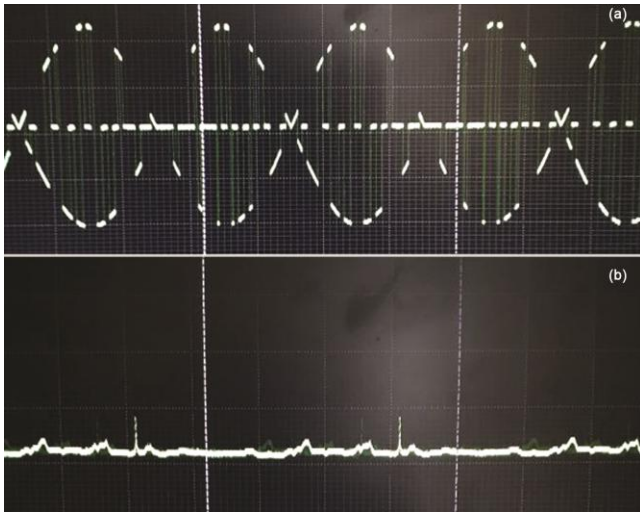

Fig. 14 — Real-time results of the DMC with SDM at f_o = 5 kHz: (a) o/p voltage and (b) THD waveform associated with o/p voltage.

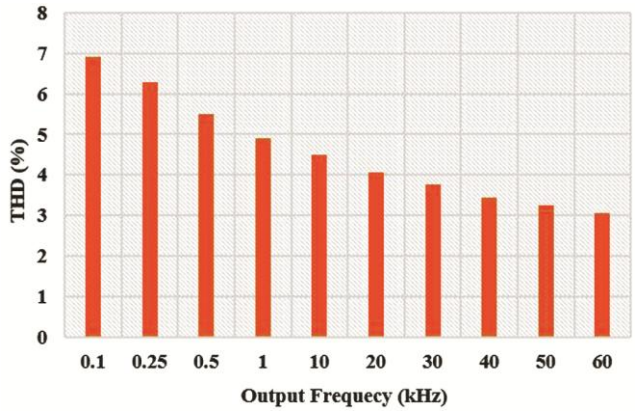

Fig. 15 — FPGA based performance analysis of the proposed DMC.

THD has been significantly minimized for the DMC with the SDM. Satisfactory working of the proposed DMC has been tested for a range of the o/p frequencies, f_o = 100 Hz to 60 kHz. The comparative performance analysis of the proposed single-phase DMC with the SDM technique for variation in o/p frequencies is illustrated in Fig. 15. A specific trend is observed for the THD values with variation in o/p frequencies for the proposed DMC; i.e., with the increment in the o/p frequency, the THD reduces significantly.

7 Conclusions

(i) A digital controller for the proposed single-phase direct matrix converter (DMC) has been developed with the help of a real-time digital simulator, "OPAL-RT: OP4510 (utilizing Kintex-7 FPGA)", which produces the modulated firing pulses applied to different IGBT switches employed in the DMC. There by, generating the o/p voltage, varying with the higher frequencies than the i/p frequency. An advanced modulation technique, Sigma-Delta modulation (SDM) has successfully been implemented for reducing the THD associated with the output voltage.

(ii) Functioning of the DMC has also been simulated on SIMULINK/ MATLAB platform followed by the real-time validation and fruitful verification for o/p frequency range of 100 Hz to 60 kHz. Satisfactory operations, of the DMC have been successfully demonstrated for both the verifications. It is observed with the SDM that, the THD associated with the o/p voltage of the DMC is obtained as low as around 3.1 %.

(iii) The developed DMC can be used for many applications, eg. Wind energy conversion systems, as the primary converter, for high frequency (HF) conversion applications in the contact-less charging of electrical vehicles and as the HF isolated grid-connected converter for battery energy storage system.

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