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Temperature dependence of *J–V* and *C–V* characteristics of *n*-InAs/*p*-GaAs heterojunctions prepared by flash evaporation technique and liquid phase epitaxy

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In this work, *n*-type of InAs films have been successfully fabricated on *p*-GaAs monocrystalline substrates by both flash evaporation technique and liquid phase epitaxy. The elemental composition of the prepared films has been confirmed by energy dispersive X-ray (EDX) spectroscopy. The morphology of the films has been characterized by scanning electron microscopy (SEM). The current transport mechanisms of *n*-InAs/*p*-GaAs heterojunctions in the temperature range 300-400 K have been investigated. Temperature-dependent dark current density-voltage (*J–V*) studies under forward and reverse bias have been carried out for this purpose. In the temperature range studied, the dark current contribution in the low bias range is believed to be due to the generation-recombination of minority carriers in the space-charge region. A change in the preparation technique does not seem to have altered the dark current conduction mechanism. Capacitance-voltage (*C–V*) at various temperatures has been measured to identify the junction type as well as determination of the important junction parameters.

Keyword: Liquid phase epitaxy, Flash evaporation, *n*-InAs/*p*-GaAs heterojunctions

1 Introduction

It is well known that InAs is a direct-gap semiconductor with a small optical band gap of 0.35 eV and large effective-mass ratio between electrons and heavy holes[1]. For application in electronic devices, InAs thin layers must be grown on semi-insulating substrates to prevent current leakage, but no suitable lattice-matched semi-insulating substrate exists for InAs. Gombia *et al.*[2] prepared Au/ GaAs/ InAs(QD)/ GaAs Schottky barriers as well as ohmic/GaAs/InAs(QD)/GaAs/ohmic structures by atomic layer molecular beam epitaxy (ALMBE) and studied the electrical properties of these structures. They have investigated the electrical properties by space charge spectroscopy techniques, current–voltage and capacitance-voltage measurements. Tangmettajittakul *et al.*[3] have compared the spectral response and band edge of three Schottky devices of InAs/GaAs, prepared by molecular beam epitaxy. However, to the best of our knowledge, there is little reported on the growth of such heterostructure by flash evaporation, FE technique as well as liquid phase epitaxy, LPE. Here we report the growth of InAs/GaAs heterostructure employing both FE technique and LPE wherein we have overcome many of the problems associated with the growth by optimizing several junction parameters such as series resistance, ideality factor, and barrier height and built-in potential. In this paper, in order to achieve a better understand of the *n*-InAs/*p*-GaAs heterojunction prepared by both flash evaporation and liquid phase epitaxy, the structural and electrical properties of the two prepared devices are compared. The current-voltage and capacitance-voltage characteristics in dark at different temperatures were measured and discussed.

2 Experimental Details

2.1 Fabrication of *n*-InAs/*p*-GaAs heterojunction

p-type GaAs wafer with (100) orientation and $\rho = 5–10\ \Omega$.cm resistivity was used as substrate in this study. The substrate was chemically cleaned using the RCA cleaning procedure (i.e., boiling in $NH_4+H_2O_2+6H_2O$ for 10 min followed by a 10 min boiling in $HCl+H_2O_2+6H_2O$). Thin films of InAs were prepared on GaAs by flash evaporation technique and liquid phase epitaxy. The flash evaporation technique was performed under 10^{-4} Pa onto pre-cleaned GaAs

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substrates held at a temperature 300 K using a high vacuum coating unit (Edwards E 306 A, England). The flash evaporation attachment was nearly similar to that described elsewhere[4].

The technique of LPE is described in detail elsewhere[5,6]. The loaded boat was heated up to 850 K and kept at this temperature for 30 min to homogenize the solution and then cooled down to 300 K with a cooling rate of 10 K/min. The growth process is terminated by removing the ready substrate with its upper layer from the solution cell.

2.2 Characterization techniques

The film morphology was investigated by scanning electron microscopy (SEM) using Model SEM model JEOL JXA-8400 A. EDX Unit is attached to with this model, with accelerating voltage 30 kV.

X-ray diffraction measurements have been taken by using analytical X'Pert PRO MRD diffractometer system having CuK_{α}, as a radiation source of wavelength $\lambda = 1.540598$ Å with $2\theta = 30°–90°$ at the scan speed 0.5 K/min for the determination of *n*-InAs/*p*-GaAs heterojunction. The analysis has been performed by using Powder Software.

Ge/Ni/Au electrode was first evaporated on InAs through suitable mask to form a front ohmic electrode and other Au/Zn/Au contact was evaporated on GaAs as back electrode, so as to form InAs/GaAs heterojunction. In order to measure the electrical properties of the heterojunction, electrical contacts were equipped with copper wires mechanically applied to the two metal electrodes using thermosetting silver paint. The dark current-voltage (*I–V*) measurements were performed at different temperatures by a high impedance programmable Keithley 617 source meter. The dark capacitance-voltage measurements were performed at different temperatures by maintaining a constant fixed frequency at 1 MHz, using a computerized capacitance–voltage system consisting of the 410 *C–V* meter via model 4108 *C–V* interface. The temperature was measured directly by means of chromel–alumel thermocouple connected to hand-held digital thermometer. Sketch of *n*-InAs/*p*-GaAs heterojunction and its electrical measurements is shown in Fig. 1.

3 Results and Discussion

3.1 Morphology characterization

SEM micrograph of *n*-InAs/*p*-GaAs prepared by LPE and flash evaporation technique is shown in the inset of Fig. 2(a,b). These figures show a nearly homogenous, without cracks or pinholes and well cover to the substrate for the films prepared by the two methods. Moreover, small nano-sized grains are uniformly distributed over smooth back-ground for the films prepared by flash evaporation as compared to those prepared by LPE. This clearly indicates that the nanocrystalline nature of film prepared by flash evaporation is highly smooth and fine as compared with those obtained by LPE.

3.2 Composition characterization

The EDX spectral analysis for the *n*-InAs/*p*-GaAs prepared by flash evaporation technique and liquid phase epitaxy are shown in Fig. 2(a,b). Fully quantitative analysis results were obtained from the spectrum by processing the data through a correction program and given in Table 1. The obtained percentages of the constituent elements in all investigated films

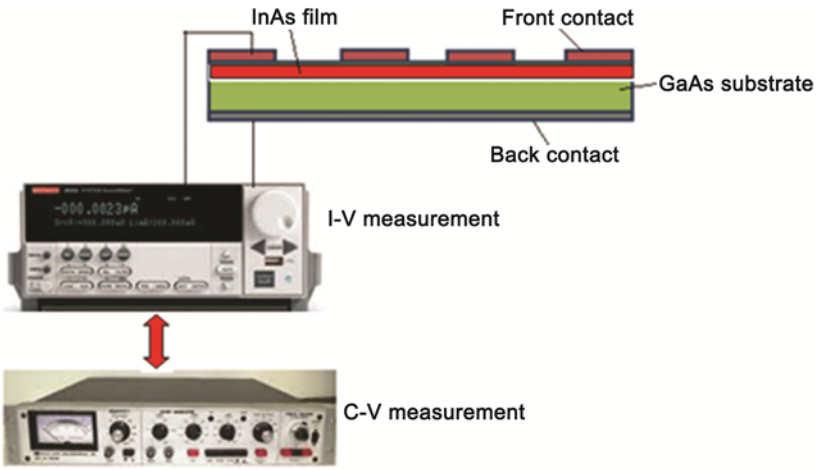

Fig. 1 — Sketch of *n*-InAs/*p*-GaAs heterojunction and its electrical measurements.

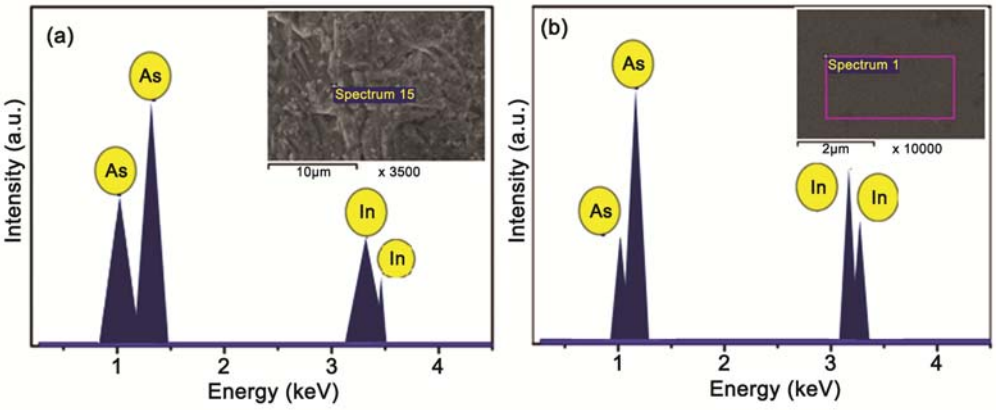

Fig. 2 — (a) EDX spectrum of *n*-InAs/*p*-GaAs prepared by LPE (the inset shows SEM image) and (b) EDX spectrum of *n*-InAs/*p*-GaAs prepared by flash evaporation (the inset shows SEM image).

Table 1 — EDX results of InAs prepared by flash evaporation and LPE techniques.

	Flash		LPE	
Element	Weight %	Atomic%	Weight %	Atomic%
In(L)	60.52%	49.9%	60.520%	49.6%
As(K)	39.48%	50.1%	39.480%	50.4%
Total	100%	100%	100%	100%

indicate that samples prepared by the two methods are nearly stoichiometric. The obtained results give support for the quality of the prepared InAs films by flash evaporation technique as compared to that of prepared by liquid phase epitaxy.

3.3 Crystalline characteristics

The X-ray diffraction patterns, XRD of the *n*-InAs/*p*-GaAs heterojunction prepared by LPE and flash evaporation are shown in Fig. 3(a,b). The presented patterns were recorded at an incident angle 2θ =5° and then do not show any diffraction peaks for the GaAs substrate. It is observed that the crystalline structure of the InAs film prepared by liquid phase epitaxial is highly oriented due to high crystallinity characteristics as compared with those prepared by flash evaporation. A flash evaporated film shows a low crystallinity since few well-resolved peaks were observed over a wide base that corresponds to cubic phase of InAs. The lattices mismatch[8] between InAs and GaAs is ~7%. Thus, epitaxial growth of distorted InAs on GaAs causes an in-plane shear strain. The diffraction peaks present in the figure are consistent with the standard JCPDS card No. 73-1983 for cubic type structure. The maximum intensity in the experimental pattern indicated by (222) plane for LPE InAs. Three preferred orientations of (111), (220) and

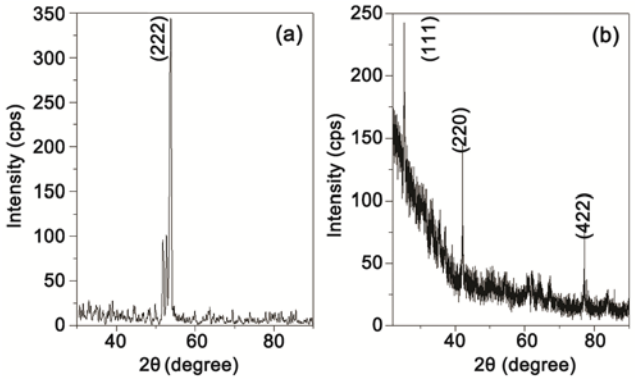

Fig. 3 — X-ray diffraction patterns of *n*-InAs/*p*-GaAs heterojunction prepared by (a) LPE and (b) flash evaporation.

(422) are characterized for the InAs film prepared by flash evaporation. All the corresponding orientations are inconsistent with the standard card which gives support for the stability of prepared InAs film.

Average crystallite size of InAs film was calculated by using Scherrer's formula[9]:

$$D = \frac{\lambda}{\beta \cos\theta} \quad \ldots (1)$$

where D is the mean crystallite size, λ is the X-ray wavelength used, β is the angular line width of half maximum intensity and θ is Bragg's diffraction angle. The mean crystallite size of InAs film prepared by LPE was found to be 28 nm and 16 nm for the film prepared by flash evaporation.

3.4 Forward *J–V* characteristics

Figure 4(a,b) shows the semi-logarithmic forward dark *J–V* plots at several temperatures in the range 300-400 K for the flashy evaporated and epitaxially grown *n*-InAs/*p*-GaAs heterojunctions. It can be seen that in both the figures, current increases

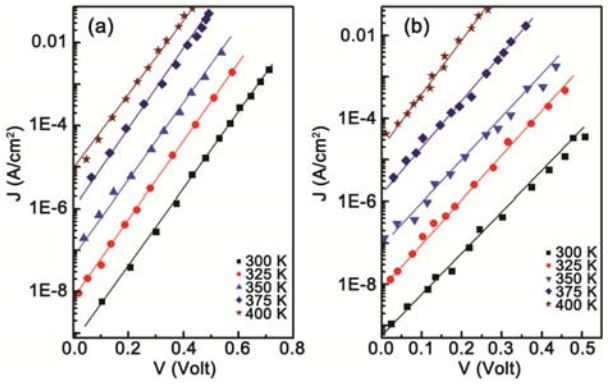

Fig. 4 — Semilogarithmic plot of forward *J-V* characteristics of *n*-InAs/*p*-GaAs prepared by (a) flash evaporation technique and (b) LPE technique.

Table 2 — Parameters deduced from *J-V* characteristics.

	LPE			Flash evaporation		
T (K)	n	R_s (Ω)	Φ_b (eV)	n	R_s (Ω)	Φ_b (eV)
300	1.79	1.77	0.67	1.77	319.5	0.54
325	1.62	1.48	0.72	1.48	297.4	0.62
350	1.59	1.31	0.76	1.31	92.58	0.67
375	1.42	1.25	0.81	1.25	40.2	0.75
400	1.29	1.1	0.85	1.1	29.9	0.84

exponentially with bias voltage. In the temperature and voltage range studied, one slope in each fitted line can be observed and then the *J–V* characteristics of a *n*-InAs/*p*-GaAs heterojunctions can be described by the expression[10]:

$$J = J_s\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad \ldots (2)$$

where n is the ideality factor, k is the Boltzmann constant, R_s is the series resistance (R_s is mostly the combined effect of bulk of the device and the barrier, for an ideal diode[11], $R_s \to 0$) and T is the absolute temperature, J_s is the device saturation current, derived from the straight-line intercept of ln$J$ at $V = 0$ and can be given by the following expression:

$$J_s = A^* T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \quad \ldots (3)$$

where A^* is the effective Richardson constant[12] taken as 8.9 A/cm^2 K^2 for *p*-GaAs and Φ_b is the barrier height which can be calculated from Eq. (3). The experimental values of Φ_b for the two junctions are given in Table 2 and plotted as a function of temperature (shown in Fig. 5). The junction prepared by flash evaporation has lower barrier height values

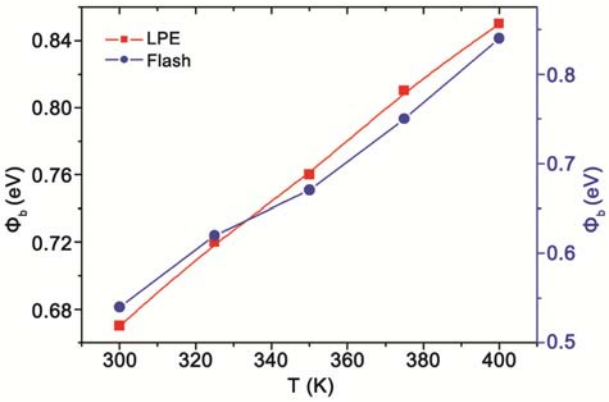

Fig. 5 — Temperature dependence of barrier height of *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

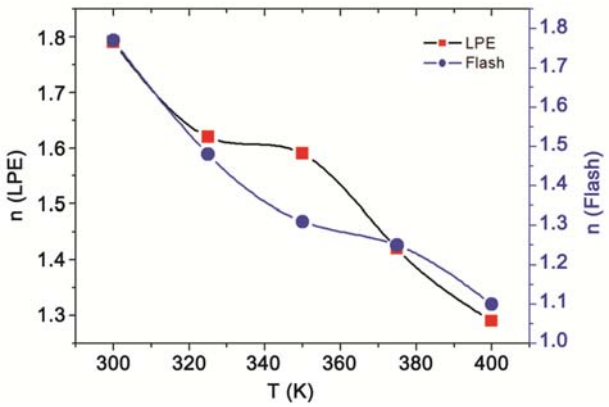

Fig. 6 — Temperature dependence of ideality factor of *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

compared with those prepared by LPE. The ideality factor (n) is obtained from the slope of the straight line region of the forward bias ln J–V plot and expressed by the following equation:

$$n = \frac{q}{kT}\exp\left(\frac{dV}{d(\ln J)}\right) \quad \ldots (4)$$

The ideality factor gives information about the recombination process that takes place in the device and shape of the interfaces[13]. The temperature dependence of ideality factor is given in Table 2 and plotted in Fig. 6. The ideality factor n approaches 2 when the generation and recombination of electron-hole pairs in the junction depletion region dominates and n equals 1 when the diffusion current dominates[13]. The values of n and J_s are evaluated from *J–V* plots by fitting the data to Eq. (1). In order to identify the dominant dark current transport mechanism, the *J–V* characteristics were examined using various conduction models. The obtained values of n lie between 1.79 at 300 K and 1.29 at 400 K for

the junctions prepared by LPE but the corresponding values for the junction prepared by flash evaporation being 2 at 300 K and 1.2 at 400 K. The values of n lying between 1 and 2 suggest that the current is due to recombination within the depletion region[9]. A plot of $\ln(J_s T^{-2.5})$ versus $1/T$ is shown in Fig. 7(a, b). The activation energy determined from such a plot should be equal to approximately half the band gap if the current is controlled by the generation-recombination in the depletion region should be close to the band gap if the current is controlled by diffusion[14]. The activation energy of the flashy evaporated junction and epitaxially junctions calculated from the slope of the ln $(J_s T^{-2.5})$ versus $1/T$ plot is found to be 0.68 and 0.74 eV, respectively, close to half the band gap of GaAs. This suggests that the generation-recombination of carriers in the depletion region determines the dark current for both flashy evaporated and epitaxial junctions. The generation-recombination component of the current does not seem to change much for the two types of preparation. LPE technique has not caused major change in the depletion region of the device.

The series resistance (R_s) of junction is important parameter for heterojunction application. For high device performance, the series resistance should be kept as low as possible. The value of R_s can be determined from the current density-voltage characteristics at sufficiently higher forward bias in the temperature range (300-400 K) which is given in Table 2 and plotted in Fig. 8 as a function of temperature. The higher series resistance can arise from the contact; the resistance of the semiconductor and the depletion layer edge[15]. Moreover, the series resistance for both junctions decreases with increasing temperature as shown in Fig. 8. This behaviour can be attributed to the increase in the number of density of the free carriers[16].

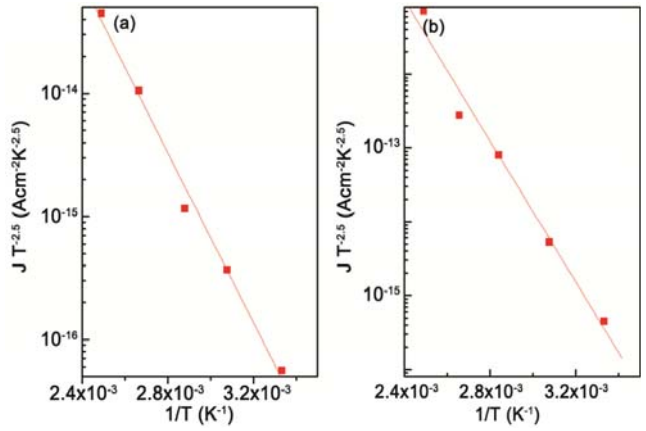

Fig. 7 — Plot of $JT^{2.5}$ versus T^{1} of *n*-InAs/*p*-GaAs heterojunction prepared by (a) flash evaporation technique and (b) LPE technique.

3.5 Reverse *J–V* characteristics

Figure 9(a,b) shows the reverse *J–V* characteristics of the flashy evaporated and epitaxially grown *n*-InAs/*p*-GaAs junctions at various temperatures in the range 300-400 K. The reverse current density-voltage characteristics indicate that the dark current is governed by generation-recombination of carriers in the depletion region. Figure 10(a,b) shows the temperature dependence of the reverse current of flashy evaporated and epitaxially junctions, respectively, plotted in the form of log (J_R) as a function of 1/T. As the Arrhenius plot appears to exhibit a thermally activated behaviour, the reverse current can be expressed as[17]:

$$J_R \alpha \exp\left(\frac{-\Delta E}{kT}\right) \quad \ldots (5)$$

where ΔE the activation energy and k is the Boltzmann constant. The activation energy calculated

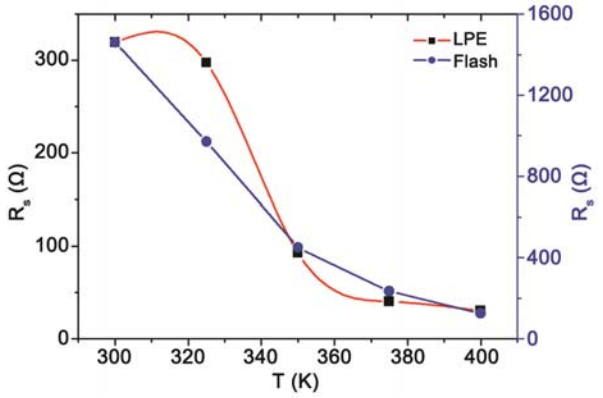

Fig. 8 — Temperature dependenceof series resistance of *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

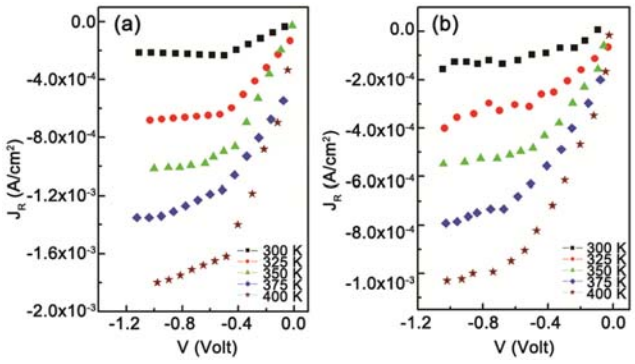

Fig. 9 — Semilogarithmic plot of J_R-V characteristics of *n*-InAs/*p*-GaAs prepared by (a) flash evaporation technique and (b) LPE technique.

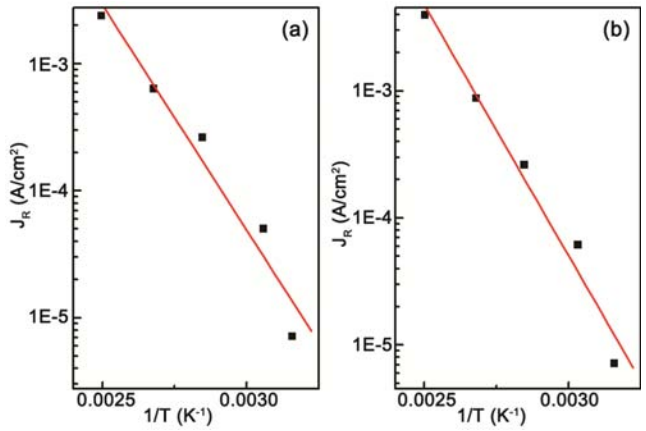

Fig. 10 — Plot of J_R versus T^{-1} of *n*-InAs/*p*-GaAs heterojunction prepared by (a) flash evaporation technique and (b) LPE technique.

from the Arrhenius plot of the reverse current at 1 V are 0.76 and 0.7 eV for the flashy evaporated and epitaxially grown junctions, respectively. These values are close to $E_g/2$. This confirms that the reverse current is dominated by the carrier recombination at the depletion region in the studied temperature range[17,18].

3.6 Capacitance-voltage characteristics

The dark capacitance-voltage characteristics of the flashy evaporated and epitaxially grown *n*-InAs/*p*-GaAs junctions are studied at various temperatures in the range 300-400 K at 1 MHz. This frequency is high enough to neglect the dielectric relaxation process in InAs film[16] and get information on the depletion region extended in the *p*-GaAs side.

The depletion layer capacitance of a junction at a voltage V is given by[19]:

$$C^{-2} = \frac{2(V_b + V)}{q\varepsilon_s\varepsilon_o A^2 N} \quad \ldots (6)$$

where A is the effective diode area, N is the carrier concentration, ε_s is the dielectric constant of GaAs, ε_0 is the vacuum permittivity and V_b is the built-in potential. Figures 11(a,b) and 12(a,b) show the dependence of $1/C^2$ on voltage at various temperatures. $1/C^2$–V plots for *n*-InAs/*p*-GaAs heterojunctions are linear for the two prepared samples in the measured temperature range. All these indicate that abrupt junction is formed in the flashy evaporated and epitaxially grown junctions[13,14]. According to Eq. (3), the net carrier concentration and the built-in potential are obtained from the slope and the intercept of the straight line of $1/C^2$–V plots, respectively and plotted as a function of temperature as shown in Figs 13 and 14. The net carrier

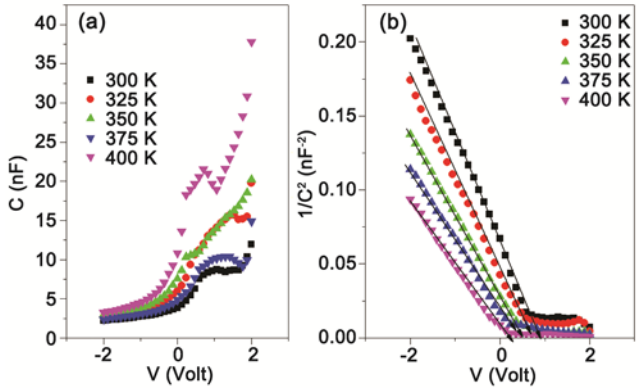

Fig. 11 — Plot of (a) *C*-*V* characteristics and (b) C^{-2}-*V* characteristics at different temperatures of *n*-InAs/*p*-GaAs prepared by flash evaporation technique.

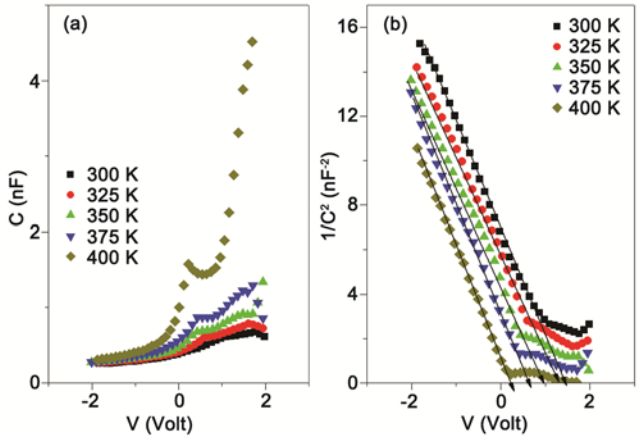

Fig. 12 — Plot of (a) *C*-*V* characteristics and (b) C^{-2}-*V* characteristics at different temperatures of *n*-InAs/*p*-GaAs prepared by LPE technique.

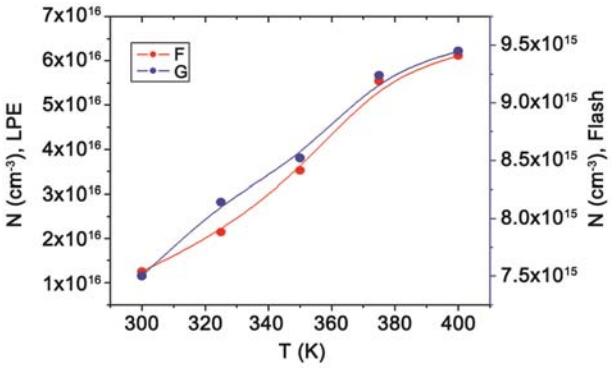

Fig. 13 — Temperature dependence of N for *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

concentration was also obtained as shown in Fig. 13 and given in Table 3 as a function of temperature. The net carrier concentration obtained from the *C*–*V* characteristics is found to increase with increasing of temperature. High values of V_b for InAs/*p*-GaAs heterojunctions prepared by LPE as compared to

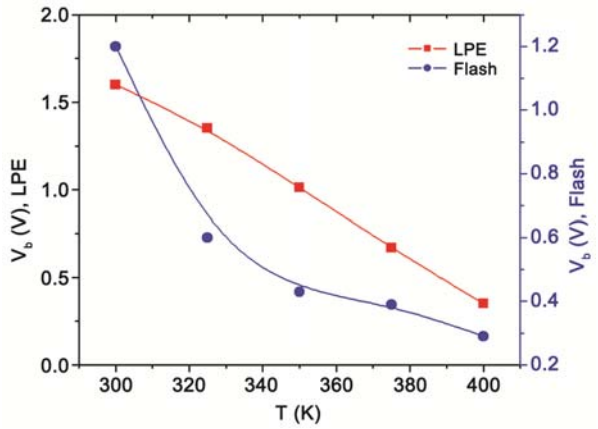

Fig. 14 — Temperature dependence of V_b for *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

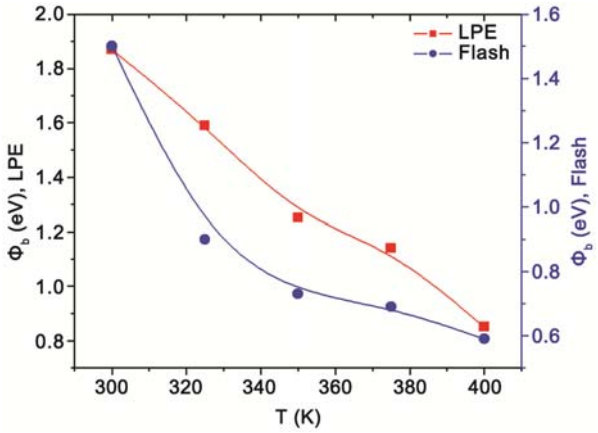

Fig. 15 — Temperature dependence of Φ_b for *n*-InAs/*p*-GaAs prepared by flash evaporation technique and LPE technique.

Table 3 — Parameters deduced from *C-V* characteristics.

LPE				Flash evaporation		
T (K)	V_b (V)	Φ_b (eV)	N_a ($\times 10^{16}$ cm^{-3})	V_b (eV)	Φ_b (eV)	N_a ($\times 10^{15}$ cm^{-3})
300	1.60	1.87	1.25	1.20	1.50	7.50
325	1.35	1.59	2.14	0.60	0.90	8.14
350	1.01	1.25	3.52	0.43	0.73	8.52
375	0.67	1.14	5.54	0.39	0.69	9.24
400	0.35	0.85	6.12	0.29	0.59	9.45

those prepared by flash evaporation (especially for the lower temperature range) may be attributed to the dependence of built-in potential on the device fabrication processes[20]. The barrier height can easily derived from built-in potential and plotted as a function of temperature as shown in Fig. 15 and given in Table 3. As observed, the barrier height obtained from *C–V* measurement is higher than those obtained from *J–V* measurement. The discrepancy between these values can be attributed to the existence of excess capacitance at the structure or presence of barrier inhomogeneities takes place[21].

4 Conclusions

The dark current characteristics of *n*-InAs/*p*-GaAs heterojunctions prepared by flash evaporation and liquid phase epitaxy were studied systematically as a function of applied bias voltage and temperature. The dark current contribution at low bias, in the measured temperature range, is due to the generation-recombination of minority carriers in the depletion region. Different preparation techniques do not seem to have changed the generation-recombination component of the dark current. Capacitance-voltage measurements indicate abrupt junction which is formed in *n*-InAs/*p*-GaAs heterojunctions prepared by flash evaporation and liquid phase epitaxy. Barrier height value obtained from *C–V* measurements is higher than those obtained from *J–V* measurements.

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