Indian Journal of Pure & Applied Physics Vol. 52, APril 2014, pp. 277-283

# CCCIIs-based sinusoidal quadrature oscillators with non-interactive control of condition and frequency

Saksit Summart<sup>1</sup>\*, Chanchai Thongsopa<sup>1</sup> & Winai Jaikla<sup>2</sup>

<sup>1</sup>School of Telecommunication Engineering, Suranaree University of Technology, Thailand

<sup>2</sup>Department of Engineering Education, Faculty of Industrial Education,

King Mongkut's Institute of Technology Ladkrabang, Thailand

\*E-mail: ton3555@hotmail.com

Received 1 March 2013; revised 25 September 2013; accepted 22 January 2014

The paper presents two current-mode quadrature oscillators with non-interactive two current controls for both of the condition of oscillation (CO) and the frequency of oscillation (FO) using current controlled current conveyors (CCCIIs). The proposed oscillators can provide two sinusoidal output currents with 90 degrees phase difference. It also provides high output impedances that make the circuit can directly drive load without additional current buffer. The condition of oscillation and frequency of oscillation can be controlled by adjusting the bias currents of the CCCIIs. The proposed circuits use only grounded capacitors without any external resistor which is very appropriate for further development into an integrated circuit. The results of PSPICE simulation program are corresponding to the theoretical analysis.

Keywords: Current-mode, Quadrature oscillator, High output impedance, Non-interactive control, CCCII

### **1** Introduction

Quadrature oscillator (QO) is one of oscillator circuit which provides two sinusoidal signals with 90° phase difference. The quadrature signal is used in telecommunications for single-sideband modulators and quadrature mixers<sup>1</sup>. In the last decade, a lot of work in electronic circuit design has been presented in current-mode technique using the current-mode building block. It is stated that the circuit designed from current-mode technique can provide the advantages such as larger dynamic range, inherently wide bandwidth, higher slew-rate, greater linearity and low power consumption<sup>2,3</sup>. According to recent research reviews on designing current-mode quadrature oscillator circuit using active building block, it is found that the most recommended qualifications for an appropriate circuit design without additional external resistor, using grounded capacitors, providing high output impedance, and electronic control circuit etc. The second generation current conveyor (CCII) and current controlled current conveyor (CCCII) have been presented as active building block, which are suitable for a class of analog signal processing for voltage-mode and current-mode technique. From literature survey, it is found that several implementations of quadrature oscillator circuits using CCII and CCCII<sup>4-30</sup>, have been reported. Unfortunately, these reported circuits suffer from one or more of following weaknesses.

- 1 Excessively use of the passive elements, especially external resistors<sup>4-20,28,29</sup> and the proposed circuits consist of large number (more than five components) of passive components, which are not convenient in future fabrication in integrated circuits<sup>6-10,13-19,28</sup>.
- 2 The condition of oscillation and the frequency of oscillation cannot be electronically controlled by adjusting the bias current<sup>4-19</sup>.
- 3 Output impedances are not high that make the circuit cannot directly drive  $load^{5,27}$ .
- 4 The proposed circuits use floating capacitor<sup>4,12-13,16</sup>, which is not convenient in future to fabricate the integrated circuits<sup>31</sup>.
- 5 The proposed circuits are not non-interactive dualcurrent control for both the condition of oscillation and the frequency of oscillation<sup>4-14,16-19,21-30</sup>.

The proposed quadrature oscillators are compared with previously published quadrature oscillators based on second generation current controlled current conveyors; the results are presented in Table 1.

The current-mode sinusoidal quadrature oscillators based on second generation current conveyors (CCCIIs) are presented in the paper. The CO and FO can be adjusted by electronic method and noninteractive dual current control for both the CO and FO. The proposed circuits consist of four CCCIIs and two grounded capacitors without additional external resistor which are suitable to be developed into

Table 1—Comparison between various oscillator based on CCII and CCCII							
Ref	Active element	Number of active element	Non-interactive control for CO and FO	Grounded C only	Number of R+C	Electronic tune of CO and FO	Current-mode QO output
[4]	CCII	2(Fig. 4a)	no	no	2+2	no	no
		2(Fig. 4b)	no	no	0+2	no	no
[5]	CCII+buffer	3+2	no	yes	3+2	no	no
[6]	CCII	3(Fig. 1a)	no	yes	3+3	no	no
		3(Fig. 2a)	no	yes	5+3	no	no
[7]	CCCII	3	no	yes	5+2	no	no
[8]	CCII	3	no	yes	3+3	no	no
[9]	CCII	3	no	yes	3+2	no	yes
[10]	CCII	2	no	yes	3+3	no	yes
[11]	CCII	2	no	yes	2+2	no	yes
[12]	CCII	3(Fig. 1(b,c))	no	no	2+2	no	no
		2(Fig. 2c)	no	yes	2+2	no	no
		2(Fig. 2c)	no	no	2+2	no	no
[13]	CCII	2	no	no	5+3	no	yes
[14]	CCII	2	no	yes	4+2	no	no
[15]	CCII	4(Fig. 3a)	yes	yes	4+2	no	no
[16]	CCII	2	no	no	4+2	no	yes
[17]	CCII	3	no	yes	3+5	no	no
[18]	CCII	2	no	yes	5+2	no	no
[19]	CCII	3(Fig. 3)	no	yes	3+2	no	no
		3 (Fig. 4)	yes	yes	4+2	no	no
		3(Fig. 5)	no	yes	3+2	no	no
[20]	CCCII	3	yes	yes	1+2	yes	yes
[21]	CCCII+OTA	4+1	no	yes	0+2	yes	yes
[22]	CCCII	4	no	yes	0+2	yes	yes
[23]	CCCII	3	no	yes	0+2	yes	yes
[24]	CCCII	4	no	yes	0+3	yes	yes
[25]	CCCII	3	no	yes	0+3	yes	yes
[26]	CCCII	3	no	yes	0+2	yes	yes
[27]	CCCII	3	no	yes	0+2	yes	yes
[28]	CCCII	4	no	yes	4+4	yes	yes
[29]	CCCII	4	no	yes	2+4	yes	yes
[30]	CCCII	4	no	yes	0+4	yes	yes
Proposed QOs	CCCII	4	yes	yes	0+2	yes	yes

integrated circuits<sup>32,33</sup>. The proposed circuits have high output impedance appropriate for cascade connection application in current mode which is capable to directly drive load. The PSPICE simulation results are also shown, which are in correspondence with the theoretical analysis.

### **2** Basic Concept of CCCII

The characteristics of the ideal CCCII are represented by the following hybrid matrix:

$$\begin{bmatrix} I_{y} \\ V_{x} \\ I_{z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_{x} & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_{y} \\ I_{x} \\ V_{z} \end{bmatrix} \qquad \dots (1)$$

For CMOS CCCII, the resistance at the *x* terminal  $(R_x)$  can be written in Eq. (2). The symbol and equivalent circuit of the CCCII are shown in Figs 1

and 2, respectively. The CMOS implementation of CCCII is shown in Fig. 3.

$$R_{\chi} = \sqrt{\frac{1}{8kI_B}} \qquad \dots (2)$$

where

$$k = \mu_p C_{ox} \left( \frac{W}{L} \right)_{9,10} = \mu_n C_{ox} \left( \frac{W}{L} \right)_{11,12}$$
 ...(3)

 $k = \mu_n C_{ox} (W / L)$  is the physical parameter of CMOS transistor. Where  $\mu_n$  is the mobility of the carrier,  $C_{ox}$  the gate-oxide capacitance per unit area, W the effective channel width and L is the effective channel length.

# **3** Proposed Current-mode Quadrature Oscillator

The proposed current-mode oscillators can be shown in Fig. 4(a and b). The proposed circuits



Fig. 1 — Symbol of the CCCII



Fig. 2 — Equivalent circuit of the CCCII



Fig. 3 — Internal construction of CCCII

consist of 4 CCCIIs and 2 grounded capacitors. It is found that the output currents are flowed from the high output impedances (z port) which facilitate to cascade in current-mode circuit without the use of a buffering device. The characteristic equation of the proposed circuit is written as:

$$s^{2} + s \left( \frac{2R_{x4} - R_{x3}}{2R_{x1}R_{x4}C_{1}} \right) + \frac{1}{C_{1}C_{2}R_{x1}R_{x2}} = 0 \qquad \dots (4)$$

From Eq. (4), the condition of oscillations and frequency of oscillation are written as:

CO: 
$$2R_{x4} = R_{x3}$$
 ...(5)

and

$$FO: \omega_{osc} = \sqrt{\frac{1}{R_{x1}R_{x2}C_1C_2}} \qquad \dots (6)$$



Fig. 4 — Proposed current-mode quadrature oscillators

It is found from Eqs (5 and 6), the conditions of oscillation and frequency of oscillation are as follows:

$$CO: 2I_{B3} = I_{B4} \qquad \dots (7)$$

and

FO: 
$$\omega_{osc} = \sqrt{\frac{8k(I_{B1}I_{B2})^{\frac{1}{2}}}{C_1C_2}}$$
 ...(8)

From Eqs (7) and (8), it can be found that the condition of oscillation can be adjusted independently from the frequency of oscillation by varying  $I_{B3}$  and  $I_{B4}$  while the frequency of oscillation can be adjusted by  $I_{B1}$  and  $I_{B2}$  without disturbing the condition of oscillation. Moreover, it should be remarked that the proposed circuit enables non-interactive dual-current control for both the condition of oscillation and frequency of oscillation. From circuit in Fig. 4, the current transfer functions of  $I_{o1}$  and  $I_{o2}$  is:

$$\frac{I_{o2}(s)}{I_{o1}(s)} = -\frac{1}{R_{x2}sC_2} \qquad \dots (9)$$

For sinusoidal steady state, Eq. (9) becomes:

$$\frac{I_{o2}(j\omega)}{I_{o1}(j\omega)} = \frac{j}{R_{x2}\omega_{osc}C_2} = \frac{e^{j90^{\circ}}}{R_{x2}\omega_{osc}C_2} \qquad \dots (10)$$

It is seen from Eq. (10) that the proposed currentmode oscillators can provide 2 sinusoidal signal output currents with 90° phase difference. Sensitivities of the active and passive of oscillator circuit are shown in Eq. (11).

$$S_{R_{x1},R_{x2},C_{1},C_{2}}^{\omega_{osc}} = -\frac{1}{2} \qquad \dots (11)$$

### 4 Analysis of Non-ideal Case

For non-ideality case, the characteristic equation of CCCII in Eq. (1) is written as:

$$\begin{bmatrix} I_{y} \\ V_{x} \\ I_{z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & R_{x} & 0 \\ 0 & \pm \alpha & 0 \end{bmatrix} \begin{bmatrix} V_{y} \\ I_{x} \\ V_{z} \end{bmatrix} \qquad \dots (12)$$

The parameter  $\alpha$  is the parasitic current transfer gain from x terminal to z terminal and  $\beta$  is the parasitic voltage transfer gain from y terminal to x terminal. In non-ideal case the characteristic equation, the condition of oscillation and the frequency of oscillation from Eqs (4-6) are as follows:

## Circuit 4(a):

$$\begin{cases} s^{2} + s \frac{R_{x4}(1+\alpha_{3}) - \alpha_{1}\alpha_{4}\beta_{4}R_{x3}}{R_{x1}R_{x4}C_{1}(1+\alpha_{3})} \\ + \frac{\alpha_{1}\alpha_{2}\beta_{2}}{C_{1}C_{2}R_{x1}R_{x2}} \end{cases} = 0 \qquad \dots (13)$$

$$CO: \quad R_{x4} (1+\alpha_3) = \alpha_1 \alpha_4 \beta_4 R_{x3} \qquad \dots (14)$$

and

$$FO: \quad \omega_{osc} = \sqrt{\frac{\alpha_1 \alpha_2 \beta_2}{C_1 C_2 R_{x1} R_{x2}}} \qquad \qquad \dots (15)$$

Circuit 4(b):

$$\begin{cases} s^{2} + s \frac{R_{x4}\alpha_{1}\beta_{1}(1+\alpha_{3}) - \alpha_{1}\alpha_{4}\beta_{4}R_{x3}}{R_{x1}R_{x4}C_{1}(1+\alpha_{3})} \\ + \frac{\alpha_{1}\alpha_{2}\beta_{2}}{C_{1}C_{2}R_{x1}R_{x2}} \end{cases} = 0 \qquad \dots (16)$$

$$CO: \quad R_{x4}\alpha_1\beta_1(1+\alpha_3) = \alpha_1\alpha_4\beta_4R_{x3} \qquad \qquad \dots (17)$$

and

$$FO: \quad \omega_{osc} = \sqrt{\frac{\alpha_1 \alpha_2 \beta_2}{C_1 C_2 R_{x1} R_{x2}}} \qquad \dots (18)$$

# 5 Analysis of the Parasitic Resistances and Capacitances

The parasitic resistances and capacitances of CCCII, the input *y* and output *z* terminals consist of parasitic resistances and capacitances  $R_y$ ,  $C_y$  and  $R_z$ ,  $C_z$ , respectively. The parasitic resistances and capacitances of the CCCII can be shown in Fig. 5. If the parasitic resistances at the *y* and *z* terminals are much greater than the parasitic resistances at *x* terminal ( $R_y$ ,  $R_z$  and  $R_x$ ), the characteristic equation, the condition of oscillation and the frequency of oscillation of the quadrature oscillators from Eqs (4-6) are represented as follows:

# Circuit 5(a):

$$\begin{cases} s^{3}R_{x1}R_{x2}R_{x3}R_{x4}CC^{"}C^{"} \\ +2s^{2}R_{x1}R_{x2}R_{x4}CC^{"} \\ +s^{2}R_{x2}R_{x3}R_{x4}C^{"}C^{"} + 2sR_{x2}R_{x4}C^{"} \\ +sR_{x3}R_{x4}C^{"} - sR_{x2}R_{x3}C^{"} + 2R_{x4} \end{cases} = 0 \qquad \dots (19)$$

$$CO: \quad \begin{cases} R_{x1}R_{x2}^{2}R_{x3}R_{x4}^{2}C'C^{"}C^{"}(2R_{x1}C'C^{"}) \\ +R_{x3}C^{"}C^{"} \end{pmatrix} = 2R_{x4}(2R_{x2}R_{x4}C^{"}) \\ +R_{x3}R_{x4}C^{"} - R_{x2}R_{x3}C^{"}) \end{cases} = 0 \qquad \dots (20)$$

and

$$FO: \omega_{osc} = \sqrt{\frac{2R_{x4}}{R_{x2}R_{x4}C^{"}(2R_{x1}C^{'} + R_{x3}C^{"})}} \qquad \dots (21)$$

where 
$$C = C_{z2} + C_{z4} + C_1$$
,  $C' = C_{z1} + C_{y2} + C_2$  and  
 $C'' = C_{z1} + C_{z3} + C_{y4}$   
 $y \circ C_{y} = R_{y}$   
 $x \circ R_{x}$   
 $y \circ C_{z} = R_{z}$   
 $C_{z} = R_{z}$   
 $C_{z} = R_{z}$   
 $C_{z} = R_{z}$   
 $C_{z} = R_{z}$ 

Fig. 5 —Parasitic resistances and capacitances of the CCCII

Circuit 4(b):

$$\begin{cases} s^{3}R_{x1}R_{x2}R_{x3}R_{x4}CCC^{"}C^{"} \\ +2s^{2}R_{x1}R_{x2}R_{x4}CC^{"}C^{"} \\ +s^{2}R_{x2}R_{x3}R_{x4}CC^{"}C^{"} + 2sR_{x2}R_{x4}C^{"} \\ +sR_{x3}R_{x4}C^{"} - sR_{x2}R_{x3}C^{"} + 2R_{x4} \end{cases} = 0 \qquad \dots (22)$$

$$CO: \quad \begin{cases} R_{x1}R_{x2}^{2}R_{x3}R_{x4}^{2}C^{'}C^{''}C^{''}(2R_{x1}C^{'}C^{''}) \\ +R_{x3}C^{'}C^{''} \end{pmatrix} = 2R_{x4}(2R_{x2}R_{x4}C^{''}) \\ +R_{x3}R_{x4}C^{''} - R_{x2}R_{x3}C^{''}) \end{cases} = 0 \qquad \dots (23)$$

and

FO: 
$$\omega_{osc} = \sqrt{\frac{2R_{x4}}{R_{x2}R_{x4}C^{"}(2R_{x1}C^{'}+R_{x3}C^{"})}}$$
 ...(24)

where  $C' = C_{y1} + C_{z1} + C_{z2} + C_{z4}$ ,  $C'' = C_{z1} + C_{y2} + C_{2}$ and  $C''' = C_{z1} + C_{z3} + C_{y4}$ 

# **6** Simulation Results

To verify the theoretical prediction of the proposed current-mode quadrature oscillator in Fig. 4 (for example, proposed quarature oscillator in Fig. 4(a), the PSPICE simulation was built with  $C_1=C_2=0.5$  nF,  $I_{B1} = I_{B2} 300 \ \mu A$ ,  $I_{B3} = 15 \ \mu A$  and  $I_{B4} = 30 \ \mu A$ . The CMOS implementation of the internal construction of CCCII used in simulation is shown in Fig. 3. The PMOS and NMOS transistors employed in the proposed circuit were simulated by using the parameters of 0.35  $\mu$ A TSMC CMOS technology<sup>34</sup>. The ratio of dimension of the transistors PMOS and NMOS is presented in Table 2. The circuit was biased with  $\pm 2.5$  V supply voltages. This yields oscillation frequency of 1.0621 MHz, where the calculated value of this parameter from Eq. (8) yields 1.1782 MHz (deviated by 9.854%). This is affected by CMOS implementation used in the circuit deviated from the non-ideal properties and the effect of parasitic

Table 2—Dimensions of CMOS transistors				
Transistor	W(µm)	L(µm)		
M1, M3, M13-M15	10	0.35		
M2, M4-M8	5	0.35		
M9-M10	30	0.35		
M11-M12	10	0.35		
M16-M19	15	0.35		

elements. Figures 6 and 7 show the simulated quadrature output waveforms during initial state and steady state, respectively. Figure 8 shows the simulation result of output spectrum. The results of the harmonics distortion analysis are presented in Tables 3 and 4, where the total harmonic distortions

Table 3 — Total harmonic distortion analysis of $I_{o1}$					
Harmonic	Frequency	Fourier	Phase		
no.	(Hz)	Component (A)	(Degrees)		
1	$1.062 \times 10^{6}$	$6.675 \times 10^{-4}$	$-1.390 \times 10^{2}$		
2	$2.124 \times 10^{6}$	$4.951 \times 10^{-6}$	$2.314 \times 10^{1}$		
3	$3.186 \times 10^{6}$	$1.129 \times 10^{-5}$	$-1.207 \times 10^{2}$		
4	$4.248 \times 10^{6}$	$8.169 \times 10^{-7}$	$3.030 \times 10^{0}$		
5	$5.311 \times 10^{6}$	$2.132 \times 10^{-6}$	$-6.386 \times 10^{1}$		
6	$6.373 \times 10^{6}$	$4.908 \times 10^{-7}$	$3.665 \times 10^{1}$		
7	$7.435 \times 10^{6}$	$6.597 \times 10^{-7}$	$2.123 \times 10^{0}$		
8	$8.497 \times 10^{6}$	$8.185 \times 10^{-8}$	$-1.080 \times 10^{2}$		
9	$9.559 \times 10^{6}$	$1.180 \times 10^{-7}$	$1.412 \times 10^{1}$		
10	$1.062 \times 10^{7}$	$1.812 \times 10^{-7}$	$-7.426 \times 10^{1}$		
DC compon	ent =-1.293069	$\times 10^{-4}$			

Total harmonic distortion = 1.882904%







Fig. 8 — Output frequency spectrum

Table 4 — Total harmonic distortion analysis of $I_{o2}$					
Harmonic no.	Frequency (Hz)	Fourier Component (A)	Phase (Degrees)		
1	$1.062 \times 10^{6}$	$6.552 \times 10^{-4}$	$1.328 \times 10^{2}$		
2	$2.124 \times 10^{6}$	$5.421 \times 10^{-6}$	$-1.636 \times 10^{2}$		
3	$3.186 \times 10^{6}$	$7.243 \times 10^{-6}$	$6.506 \times 10^{1}$		
4	$4.248 \times 10^{6}$	$2.221 \times 10^{-7}$	$4.030 \times 10^{1}$		
5	$5.311 \times 10^{6}$	$1.351 \times 10^{-7}$	$2.767 \times 10^{1}$		
6	$6.373 \times 10^{6}$	$2.627 \times 10^{-7}$	$4.498 \times 10^{1}$		
7	$7.435 \times 10^{6}$	$2.225 \times 10^{-7}$	$8.665 \times 10^{0}$		
8	$8.497 \times 10^{6}$	$1.858 \times 10^{-7}$	$6.831 \times 10^{1}$		
9	$9.559 \times 10^{6}$	$1.502 \times 10^{-7}$	$5.165 \times 10^{1}$		
10	$1.062 \times 10^{7}$	$1.899 \times 10^{-7}$	$5.907 \times 10^{1}$		
DC component =-1.331735 $\times 10^{-4}$					
Total harmonic distortion = $1.383091\%$					



Fig. 9 — Oscillation frequencies against bias current for various capacitances when  $I_{B1}=I_{B2}$ 



Fig. 10 - Monte-Carlo Simulation of quadrature oscillator circuit

(THD) of  $I_{o1}$  and  $I_{o2}$  are about 1.882% and 1.383%, respectively. Tables 3 and 4 present the phase difference of the output current  $I_{o1}$  and  $I_{o2}$  which is about 88.2 degrees. The electronic tuning of the oscillation frequency with the bias current  $I_{B1} = I_{B2}$  for different capacitor values is shown in Fig. 9.

In addition, the stability can be proved by Mote-Carlo simulation which is the proportional to mobility parameter of CMOS transistor ( $\mu_n C_{ox}$ ) due to process by 10% deviation. The result of the simulation is shown in Fig. 10. It reveals that the proportional to mobility parameter has slightly affected on the frequency of oscillation then the frequency still remains close to 1.0621 MHz. Moreover, the simulation results of output resistance of  $I_{o1}$  and  $I_{o2}$ are about 15.392 k $\Omega$  and 15.364 k $\Omega$ , respectively.

# 7 Conclusions

The current-mode oscillators have been presented. The output circuit can provide sinusoidal signal currents with 88.2 degrees phase difference and high output impedances that are easy to drive external load without loading effect. The frequency of oscillation and condition of oscillation can be electronically adjusted with non-interactive dual-current control for both the condition of oscillation and the frequency of oscillation. The proposed circuits consist of 4 CCCIIs and 2 grounded capacitors without addition to any external resistors, which is convenient in future to fabricate the integrated circuits. In addition, the of proposed configuration could stability be confirmed by Monte-Carlo Simulation. PSPICE simulations are included to verify the theoretical analysis. Simulated and theoretical results are found to be in close agreement.

#### Acknowledgement

This work was supported by Suranaree University of Technology (SUT), the Office of the Higher Education under NRU project of Thailand and North Eastern Technological College, Thailand.

### References

- 1 Khan I A & Khawaja S, International J Electronics, 87 (2000) 1353.
- 2 Toumazou C & Lidgey F J, *Electron. Lett*, 22 (1986) 662-664.
- 3 Abuelma'atti N T & Al-zaher H A, *IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Proc*, 46 (1999) 69.
- 4 Sotner R, Hrubos Z, Slezak J & Dostal T, *Radioengineering*, 19 (2010) 446.
- 5 Sotner R, Hrubos Z, Sevcik B, Slezak J, Petrzela J & Dostal T, *Journal of Electronic Engineering*, 62 (2011) 258.

- 6 Minhaj N, International Journal of Recent Trends in Engineering, 1 (2009) 294-296.
- 7 Vosper J V & Heima M, Electronics Lett, 32 (1996) 2293.
- 8 Horng J W, Computers and Electrical Engineering, 31 (2005) 81.
- 9 Horng J W, Chou H P & Shiu I C, *IEEE International Symposium on Circuits and Systems*, (2006) 441.
- 10 Horng J W, Indian J Pure & Appl Phys, 49 (2011) 494.
- 11 Lahiri A, Analog Integrated Circuits signal Processing, 68 (2011) 129.
- 12 Lahiri A, Active and Passive Electronic Components, 2011 (2011) 1.
- 13 Un M & Kacar F, Istanbul Commerce University Journal of Science, 1 (2007) 119.
- 14 Khan A A, Bimal S, Dey K K & Roy S S, IEEE Transactions on Instrumentation and Measurement, 54 (2005) 2402.
- 15 Soliman A M, Microelectronics Journal. 41 (2010) 680.
- 16 Un M & Kacar F, Journal of Electrical & Electronics Engineering, 8 (2008) 529.
- 17 Horng J W, Hou G L, Chang C M, Pan S W, Shie J Y & Wen Y H, 6<sup>th</sup> WSEAS International Conference on Instrumentation, Measurement, Circuits & Systems, (2007) 89.
- 18 Beg P, Khan I A & Ahmed M T, International Multimedia, Signal Processing and Communication Technologies, (2009) 155.
- 19 Bumrongchoke T, Duangmalai D & Jaikla W, International Symposium on Communications and Information Technologies (ISCIT), (2010) 192.

- 20 Songkla S N, Jaikla W & Sreewirote B, 18th International Conference "Mixed Design of Integrated Circuits and Systems", (2011) 212.
- 21 Jaikla W & Siripruchyanun M, Circuits, Systems, and Signal Processing, 28 (2009) 99.
- 22 Thongjan N, Tanaphatsiri C & Siripruchyanun M, *The Seventh PSU Engineering Conference*, (2009) 250.
- 23 Ghosh M, Bhattacharya S, Ranjan A & Paul S K, Int. Colloquiums on Computer Electronics Electrical Mechanical and Civil, (2011) 142.
- 24 Maheshwari S & Khan I A, *IEE Proceedings-Circuits,* Devices and Systems, (2005) 605.
- 25 Maheshwari S, IET Circuits, Devices & Systems, 4 (2010) 188.
- 26 Lahiri A, Radioengineering, 20 (2011) 349.
- 27 Maheshwari S, Active and Passive Electronic Components, 26 (2003) 193.
- 28 Minhaj N, XXXII Nationl Systems Conference, NSC, (2008) 335.
- 29 Minhaj N, International Conference on Advances in Computing, Control, & Telecommunication Technologies, (2009) 424.
- 30 Hasan S & Khan I A, *The Arabian Journal for Science and Engineering*, 32 (2007) 127.
- 31 Yuce E & Minael S A, *IEEE Trans. On Circuit and Syst. I*, 55 (2008) 266.
- 32 Bhusan M & Newcomb R W, Electronics Letters, 3 (1969) 148.
- 33 Soliman A M, Journal of Active and Passive Electronic Devices, 3 (2008) 175.
- 34 Yuce E, International Journal of Electronics and Communications (AEU), 61 (2007) 453.