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Novel instrumentation amplifier and integrator circuits using single DDCC and only grounded passive elements

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In the present paper, very simple voltage-mode instrumentation amplifier (IA) and integrator structures including only grounded passive components yielding easy integration are proposed. The proposed IA and integrator use single differential difference current conveyor. The proposed IA without requiring critical passive component matching conditions can be constructed with only two small-valued resistors to obtain high gain. The proposed integrator circuit has the feature of improved low frequency performance, which can be accomplished via a resistive component matching constraint. Also, both of the proposed circuits have high input impedances yielding easy cascadability. Both of the proposed configurations consume less power, and can be operated at higher frequencies. Some simulation and experimental results are included to confirm the theory.

Keywords: Differential difference current conveyor, Instrumentation amplifier, Integrator, Grounded passive components

1 Introduction

A differential difference current conveyor (DDCC) as a current-mode (CM) active element has the advantages of both of the second-generation current conveyor (CCII) such as wider bandwidth, greater linearity, larger dynamic range and differential difference amplifier (DDA) such as high-input impedance and arithmetic operation capability[1]. Also, DDCC was firstly proposed[2]. Instrumentation amplifiers (IAs) are widely used in many areas for example medical instrumentation, data acquisition and signal processing applications[3-13]. The IA structures consist of some active components for instance operational amplifiers[3] (OAs), operational transconductance amplifiers[4] (OTAs), current feedback operational amplifiers[5] (CFOAs), second-generation current controlled current conveyors[6] (CCCIIs) and other active elements[7-15]. In addition, a CMOS based CM IA has been proposed recently[16]. Nevertheless, all of the IA configurations[3-14] have large-valued resistors to obtain high gains. Also, IA proposed[15] is made up of a number of CMOS transistors, two floating resistors and a floating capacitor.

Active RC integrator circuits having well-established status in the areas of microelectronic circuits and systems can be applicable to active filters, process controller design, waveform generation, and calibration circuits[17,18]. However, both of the integrator circuits[17,18] do not have features of improved low frequency performance.

In the present paper, very simple voltage-mode (VM) IA and integrator topologies composed of only grounded passive components resulting in easy integration[19-21] are proposed. The proposed IA and integrator use single DDCC. The proposed IA without requiring critical passive element matching constraints can be constructed with only two small-valued resistors to obtain high gain. The proposed integrator circuit has the property of improved low frequency performance, which can be achieved by a resistive component matching condition. Both of the proposed IA and integrator structures have the properties of high input impedance resulting in easy cascadability with other VM circuits. Electronically tunable grounded resistors[22-25] can be replaced instead of the grounded resistors of the proposed IA and integrator circuits to control externally in integrated circuit (IC) technology. Both of the proposed IA and integrator circuits have only resistors but no capacitors connected in series to the X terminal of the DDCC. Consequently, both of the proposed circuits can be operated at high frequencies[26]. Some simulation and experimental results are included to verify the theory.

2 Instrumentation Amplifier Topology

The defining matrix equation of the DDCC shown in Fig. 1 can be given by:

$$\begin{bmatrix} I_z \\ I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \end{bmatrix} = \begin{bmatrix} \alpha & 0 & 0 & 0 & sC_z + 1/R_z \\ 0 & sC_{y1} & 0 & 0 & 0 \\ 0 & 0 & sC_{y2} & 0 & 0 \\ 0 & 0 & 0 & sC_{y3} & 0 \\ R_x + sL_x & \beta_1 & -\beta_2 & \beta_3 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_{y1} \\ V_{y2} \\ V_{y3} \\ V_z \end{bmatrix} \quad \ldots(1)$$

In matrix Eq. (1), at sufficiently low frequencies, the frequency dependent non-ideal current gain $\alpha = 1+\varepsilon_1$ and the frequency dependent non-ideal voltage gains $\beta_j = 1+\varepsilon_{j+1}$ ($j = 1, 2, 3$) are ideally equal to unity. In addition, ε_1 and ε_{j+1}, ideally equal to zero, are respectively called as current and voltage tracking errors where $|\varepsilon_k| << 1$ ($k = 1, 2, 3, 4$). Also, the effects of L_x of the DDCC in some calculations are ignored for simplicity.

The proposed IA employing a canonical number of components and a simple[14] IA are respectively shown in Fig. 2(a and b). Applying routine analysis to the proposed IA circuit in Fig. 2(a), the output voltage is found as in the following:

$$V_{\text{out}} = (V_1 - V_2)\frac{R_2}{R_1 - R_2} \quad \ldots(2)$$

where $R_1 > R_2$ should be chosen. If only non-ideal gains are considered, Eq.(2) converts as:

$$V_{\text{out}} = (\beta_3 V_1 - \beta_2 V_2)\frac{\alpha R_2}{R_1 - \alpha\beta_1 R_2} \quad \ldots(3)$$

From Eq. (3), differential-mode gain (A_{DM}) and common-mode gain (A_{CM}) are respectively found to be as follows:

$$\text{A}_{\text{DM}} = \frac{V_{out}}{V_1 - V_2} = \frac{\beta_2 + \beta_3}{2}\frac{\alpha R_2}{R_1 - \alpha\beta_1 R_2} \quad \ldots(4)$$

where $V_2 = -V_1$

$$\text{A}_{\text{CM}} = \frac{V_{out}}{\frac{V_1 + V_2}{2}} = (\beta_3 - \beta_2)\frac{\alpha R_2}{R_1 - \alpha\beta_1 R_2} \quad \ldots(5)$$

where, $V_2 = V_1$. From Eqs (4) and (5), the common-mode rejection ratio (CMRR) is calculated as:

$$\text{CMRR} = \left|\frac{\text{A}_{\text{DM}}}{\text{A}_{\text{CM}}}\right| = \frac{1}{2}\left|\frac{\beta_2 + \beta_3}{\beta_2 - \beta_3}\right| \cong \frac{1}{|\varepsilon_3 - \varepsilon_4|} \quad \ldots(6)$$

It is seen from Eq. (6) that the CMRR is independent of gain of the IA but CMRR depends on voltage tracking errors. Not only frequency dependent

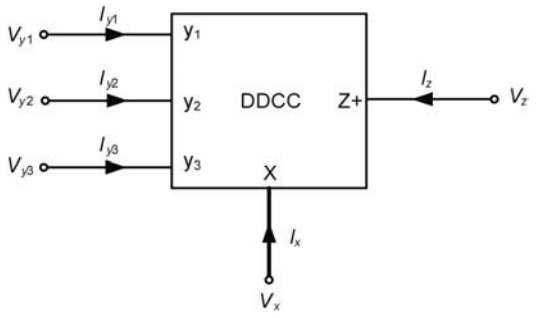

Fig. 1 — Electrical symbol of the DDCC

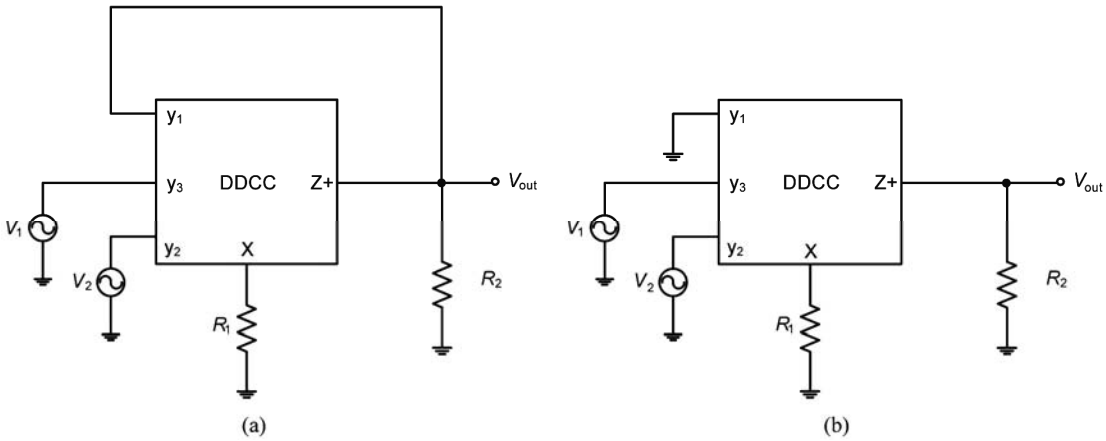

Fig. 2 — (a) Proposed voltage-mode instrumentation amplifier (b) Simple instrumentation amplifier[14]

non-ideal gains but also parasitic impedances of the DDCC affect the bandwidth of the presented topology in Fig. 2. Using a single pole model for the frequency dependent non-ideal gains[27], the following models are obtained:

$$\alpha = \frac{1+\varepsilon_1}{1+\dfrac{j\omega}{\omega_\alpha}} \qquad \ldots(7)$$

$$\beta_j = \frac{1+\varepsilon_{j+1}}{1+\dfrac{j\omega}{\omega_{\beta j}}} \qquad \ldots(8)$$

where ω_α and $\omega_{\beta j}$ (j = 1, 2, 3), ideally equal to infinity, are poles of the non-ideal current and voltage gains, respectively. Therefore, CMRR in Eq. (6) turns to:

$$\begin{aligned}\text{CMRR} &= \frac{1}{2}\left|\frac{\beta_2+\beta_3}{\beta_2-\beta_3}\right| = \frac{1}{2}\left|\frac{\dfrac{1+\varepsilon_3}{1+\dfrac{j\omega}{\omega_{\beta2}}}+\dfrac{1+\varepsilon_4}{1+\dfrac{j\omega}{\omega_{\beta3}}}}{\dfrac{1+\varepsilon_3}{1+\dfrac{j\omega}{\omega_{\beta2}}}-\dfrac{1+\varepsilon_4}{1+\dfrac{j\omega}{\omega_{\beta3}}}}\right| \\ &= \frac{1}{2}\left|\frac{2+\varepsilon_3+\varepsilon_4+\dfrac{j\omega(1+\varepsilon_4)}{\omega_{\beta2}}+\dfrac{j\omega(1+\varepsilon_3)}{\omega_{\beta3}}}{\varepsilon_3-\varepsilon_4+\dfrac{j\omega(1+\varepsilon_3)}{\omega_{\beta3}}-\dfrac{j\omega(1+\varepsilon_4)}{\omega_{\beta2}}}\right|\end{aligned} \qquad \ldots(9)$$

If only parasitic impedances except L_x of the DDCC is taken into account, Eq. (2) turns to:

$$\begin{aligned}V_{out} &= (V_1-V_2)\frac{R_2//R_z//(1/sC_{zy})}{R_1+R_x-R_2//R_z//(1/sC_{zy})} \\ &= (V_1-V_2)A_v\frac{1}{1+\dfrac{s}{\omega_c}}\end{aligned} \qquad \ldots(10)$$

where $C_{zy} = C_z + C_{y1}$ and

$$A_v = \frac{R_2//R_z}{R_1+R_x-R_2//R_z} \qquad \ldots(11)$$

is the gain of the IA.

$$\omega_c = \frac{R_1+R_x-R_2//R_z}{C_{zy}(R_1+R_x)(R_2//R_z)} \qquad \ldots(12)$$

ideally equal to infinity, is the pole frequency of the IA due to parallel Z terminal parasitic impedances and series X terminal parasitic resistor effects. Further, $A_v\omega_c$ is the gain bandwidth product of the IA where the values of A_v and ω_c depend on the values of selected passive components and parasitic impedances. Parasitic impedances of the DDCC also affect CMRR given in Eq. (9). If both parasitic impedances except L_x and frequency dependent non-ideal gains are taken into account, Eq. (2) turns to:

$$V_{\text{out}} = \alpha(\beta_3V_1-\beta_2V_2)\frac{R_2//R_z//(1/sC_{zy})}{R_1+R_x-\alpha\beta_1(R_2//R_z//(1/sC_{zy}))} \qquad \ldots(13)$$

If the effects of L_x are also considered, Eq. (10) turns to:

$$\begin{aligned}V_{\text{out}} &= (V_1-V_2)\frac{R_2//R_z//(1/sC_{zy})}{R_1+R_x+sL_x-R_2//R_z//(1/sC_{zy})} \\ &= \frac{(V_1-V_2)}{s^2L_xC_{zy}+s(C_{zy}(R_1+R_x)+\dfrac{L_x}{R_2//R_z})+\dfrac{R_1+R_x}{R_2//R_z}-1}\end{aligned} \qquad \ldots(14)$$

In frequency domain following constraints should be satisfied:

$$\omega << \sqrt{\frac{\dfrac{R_1+R_x}{R_2//R_z}-1}{L_xC_{zy}}} = \omega_{\text{H1}} \qquad \ldots(15a)$$

$$\omega << \frac{\dfrac{R_1+R_x}{R_2//R_z}-1}{C_{zy}(R_1+R_x)+\dfrac{L_x}{R_2//R_z}} = \omega_{\text{H2}} \qquad \ldots(15b)$$

In Eq.(15), it is assumed that both of the angular frequencies, ω_{H1} and ω_{H2}, are far away from each other. Therefore, the useful frequency range is evaluated as follows:

$$f \le \frac{0.1}{2\pi}\min\{\omega_{\text{H1}}, \omega_{\text{H2}}\} \qquad \ldots(16)$$

If frequency dependent non-ideal gain effects are considered, the limit at high frequencies reduces.

Apart from this, the proposed IA has no limit at low frequencies.

3 Integrator Configuration

The proposed integrator circuit with reduced parasitic impedance effects and a simple integrator topology[28] are shown in Fig. 3(a and b), respectively.

Applying routine analysis to the configuration of Fig. 3(a) yields the following output voltage:

$$V_{out} = \frac{V_1 - V_2}{sCR_1 + \frac{R_1}{R_2} - 1} \quad \ldots(17)$$

In Eq. (17), $R_1 \geq R_2$ should be chosen due to stability problem[27], which is an undesired drawback. If $R_1 = R_2$ is chosen, Eq. (17) turns to:

$$V_{out} = \frac{V_1 - V_2}{sCR_1} \quad \ldots(18)$$

where, if $V_1 = 0$ is selected and V_2 is applied as input voltage, a negative lossless integrator with a time constant $\tau = CR_1$ is obtained. Similarly, if $V_2 = 0$ is selected and V_1 is applied as input voltage, a positive lossless integrator with a time constant $\tau = CR_1$ is obtained. If only frequency dependent non-ideal gains are taken into account, Eq. (17) converts:

$$V_{out} = \alpha \frac{\beta_3 V_1 - \beta_2 V_2}{sCR_1 + \frac{R_1}{R_2} - \alpha\beta_1} \quad \ldots(19)$$

If only parasitic impedances except L_x are considered, Eq. (17) converts:

$$V_{out} = \frac{V_1 - V_2}{s(C + C_{zy})(R_1 + R_x) + \frac{R_1 + R_x}{R_2 // R_z} - 1} \quad \ldots(20)$$

In Eq. (20), if $R_2//R_z = R_1+R_x$ is chosen, a lossless integrator is obtained. If both parasitic impedances except L_x and frequency dependent non-ideal gains are taken into account, Eq. (17) turns to:

$$V_{out} = \frac{\alpha(\beta_3 V_1 - \beta_2 V_2)}{s(C + C_{zy})(R_1 + R_x) + \frac{R_1 + R_x}{R_2 // R_z} - \alpha\beta_1} \quad \ldots(21)$$

If the effects of L_x are also considered, Eq. (20) turns to:

$$V_{out} = \frac{V_1 - V_2}{s^2(C+C_{zy})L_x + s\left((C+C_{zy})(R_1+R_x) + \frac{L_x}{R_2//R_z}\right) + \frac{R_1+R_x}{R_2//R_z} - 1} \quad \ldots(22)$$

In Eq. (22), if $R_2//R_z = R_1+R_x$ is chosen, Eq. (22) simplifies in frequency domain as:

$$V_{out} = \frac{V_1 - V_2}{-\omega^2(C+C_{zy})L_x + j\omega\left((C+C_{zy})(R_1+R_x) + \frac{L_x}{R_2//R_z}\right)} \quad \ldots(23)$$

If following condition is satisfied, a lossless integrator is obtained.

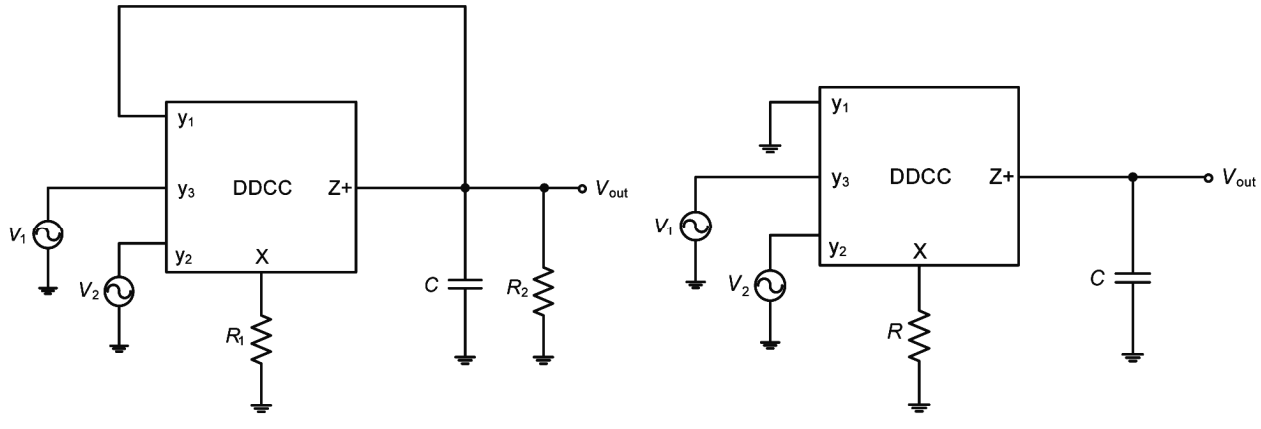

Fig. 3 — (a) Proposed voltage-mode integrator (b) Simple voltage-mode integrator[28]

$$\omega << \frac{(C+C_{zy})(R_1+R_x)+\dfrac{L_x}{R_2//R_z}}{(C+C_{zy})L_x} = \omega_H \leq 0.1\omega_H \quad \ldots(24)$$

It is understood from Eq. (24) that proposed integrator has a limit at low and high frequencies. The restriction at low frequencies stems from the Z terminal parasitic resistor[29] of the DDCC while the limitation at high frequencies is attributed to the X terminal parasitic inductor[30] of the DDCC. In Eq. (22), if $R_2//R_z = R_1+R_x$ is not satisfied, there is a limit at low frequencies as described below:

$$\omega >> \frac{\dfrac{R_1+R_x}{R_2//R_z}-1}{(C+C_{zy})(R_1+R_x)+\dfrac{L_x}{R_2//R_z}} = \omega_L \geq 10\omega_L \quad \ldots(25)$$

If only parasitic impedances are taken into account, the useful operating frequency range is found to be:

$$\frac{10}{2\pi}\omega_L \leq f \leq \frac{0.1}{2\pi}\omega_H \quad \ldots(26)$$

If frequency dependent non-ideal gain effects are considered, only the limit at high frequencies decreases whereas the restriction at low frequencies remains unchanged. It is important to note that the proposed IA and integrator circuit do not have low output impedances whereas if next stages of the proposed IA and integrator circuit are high input impedances, there is no need to use voltage followers (VFs). If it is necessary, a VF can be easily realized by employing only two MOS transistors[31]. On the other hand, integrators can be used to design analog filters[28]; accordingly, the implemented filters have the property of improved low frequency performance resulting in wider bandwidth. Furthermore, each resistor of the proposed IA and integrator can be tuned electronically by employing only two MOS transistors[25]. As a result, extra four MOS transistors are enough for each of the proposed circuits to control externally. However, the IA uses[6] three CCCIIs with tens of BJTs to control the IA electronically. On the other hand, applying routine analysis to the configurations of Fig. 2(b) and 3(b) results in the following output voltages, respectively:

$$V_{out} = \frac{R_2}{R_1}(V_1 - V_2) \quad \ldots(27a)$$

$$V_{out} = \frac{V_1 - V_2}{sCR} \quad \ldots(27b)$$

4 Simulation and Experimental Test Results

Internal structure[1] of the DDCC is shown in Fig. 4. All of the MOS transistors based on 0.13 µm IBM technology parameters[32] are operated in saturation region. All of the bulks are connected to the relevant

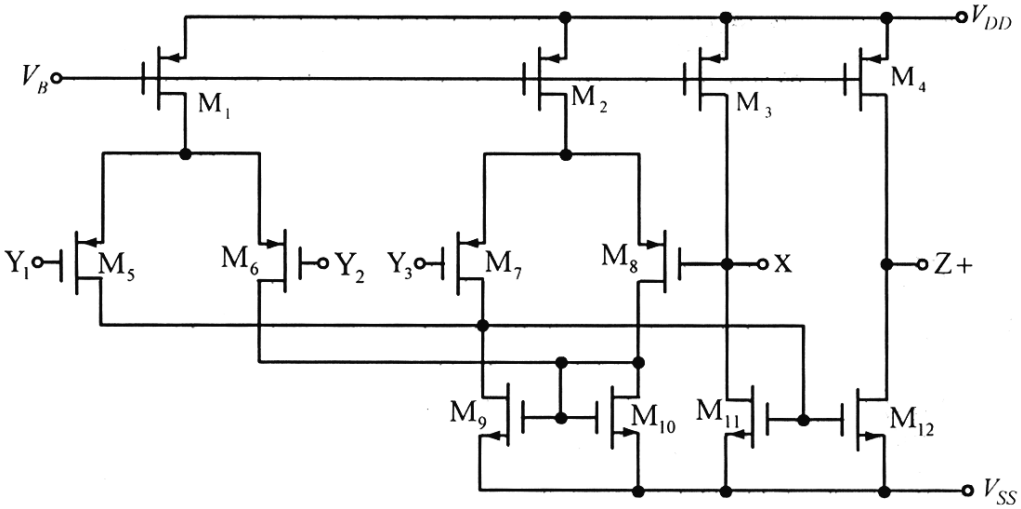

Fig. 4 — Internal structure[1] of the DDCC

sources. The dimensions of the MOS transistors are given in Table 1. The supply voltages are selected as V_{DD}=−V_{SS}=0.75 V. The bias voltage V_B is taken as 0.4 V. The parasitic impedances and parameters of the non-ideal gains of the DDCC using SPICE are computed as follows: R_x = 155.18 Ω, L_x = 2.42 µH, C_z = 11.76 fF, C_{y1} = 172.4 fF, C_{y2} = 172.4 fF, C_{y3} = 36.9 fF, R_z = 66.98 kΩ, ε_1 =-0.0033, ε_2 =-0.0014, ε_3 =–0.0022, ε_4 =–0.0014, f_α = 294 MHz, $f_{\beta1}$ = 311 MHz, $f_{\beta2}$ = 299 MHz and $f_{\beta3}$ is very large.

The passive components for the proposed IA are separately selected as R_1= 1 kΩ and R_2 = 0.8 kΩ, R_2 = 1.09 kΩ and R_2 = 1098.5 Ω to obtain gains of about 7dB, 21.5 dB and 36 dB which are shown in Fig. 5, respectively. The passive components for the proposed IA are also selected as R_1 = 1 kΩ and R_2 = 0.8 kΩ to draw CMRR which is shown in Fig. 6 where the passive components for the simple IA are chosen as R_1= 1 kΩ and R_2 = 10 kΩ. Moreover, as shown in Fig. 7, a 4mV peak to peak sinusoidal voltage signal at 5 MHz is applied to the introduced IA where the total harmonic distortion (THD) is found as 2.93% which can be acceptable. It is well-known that if symmetrical power supply voltages are increased, THD value reduces considerably. Input and output noises of the proposed IA with respect to frequency are given in Table 2. The total power consumption for the proposed IA is evaluated as 145 µW in simulations.

The passive components for the proposed integrator are selected as C=5 pF, R_1= 1 kΩ and R_2≅1058.1 Ω to obtain a time constant $\tau = CR_1=5\times10^{-9}$s. Input and output noises of the proposed integrator circuit with respect to frequency are given in Table 3. Frequency domain analysis of the developed integrator circuit is shown in Fig. 8 in which ideal, low frequency performance improved (proposed integrator) and low frequency performance unimproved (simple integrator) results are exhibited. Time domain analysis of the developed integrator circuit is shown in Fig. 9 where ideal, low frequency performance

Table 1 — Dimensions of the transistors of the DDCC+ in Fig. 4

PMOS Transistors	W(µm)/L(µm)
M_1-M_8	39/1.04
NMOS Transistors	W(µm)/L(µm)
M_9-M_{12}	13/1.04

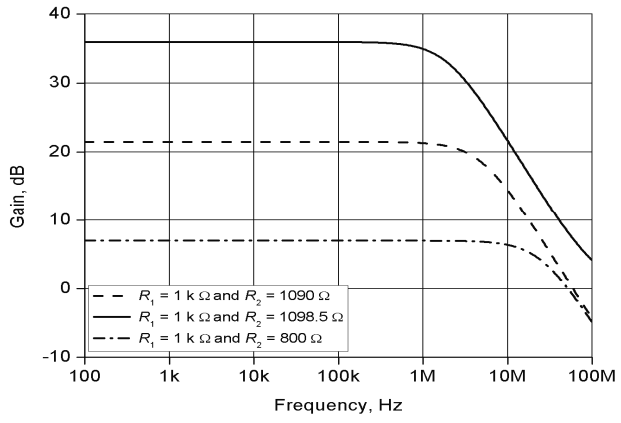

Fig. 5 — Gains of the proposed instrumentation amplifier

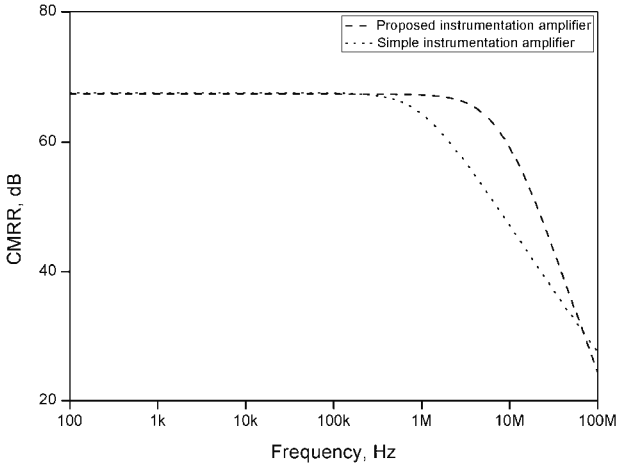

Fig. 6 — CMRRs of the proposed and simple IAs with respect to frequency

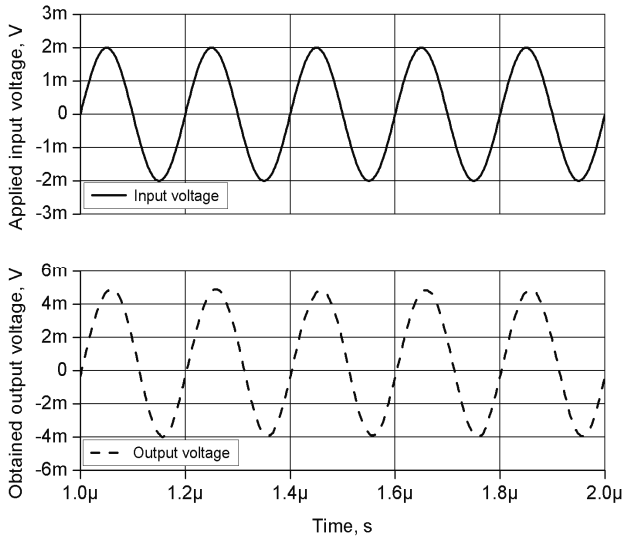

Fig. 7 — Sinusoidal input and corresponding output voltage of the proposed IA at 5 MHz

improved (proposed integrator) and low frequency performance unimproved (simple integrator) results at 50 MHz are demonstrated. Also, 150 mV peak sinusoidal voltage signal is applied to all the integrator circuits. Further, after a hundred runs, MC simulation result with 20% Gaussian deviation of the capacitor *C* as shown in Fig. 10 is achieved in which 150mV peak sinusoidal voltage signal is applied to the proposed integrator circuit. THD variations versus peak values of sinusoidal voltage signal at 50MHz are shown in Fig. 11. The total power dissipation for the proposed integrator circuit is calculated as 597μW in simulations.It is observed from simulation results from Figs 5-11 that ideal and simulation results are close to each other whereas the slight discrepancy between them can be attributed to parasitic impedances and frequency dependent non-ideal gains as discussed throughout of this paper.

Table 2 — Input and output noises of the proposed IA against frequency.

Frequency, Hz	ONOISE, V/Hz$^{1/2}$	INOISE, V/Hz$^{1/2}$
10^2	5.50×10^{-8}	2.50×10^{-8}
10^3	5.50×10^{-8}	2.50×10^{-8}
10^4	5.50×10^{-8}	2.50×10^{-8}
10^5	5.50×10^{-8}	2.50×10^{-8}
10^6	5.49×10^{-8}	2.50×10^{-8}
10^7	5.12×10^{-8}	2.46×10^{-8}
10^8	1.34×10^{-8}	2.35×10^{-8}

Table 3 — Input and output noises of the proposed integrator versus frequency

Frequency, Hz	O Noise, V/Hz$^{1/2}$	I Noise, V/Hz$^{1/2}$
10^2	6.08×10^{-5}	2.60×10^{-8}
10^3	6.05×10^{-5}	2.60×10^{-8}
10^4	4.52×10^{-5}	2.60×10^{-8}
10^5	6.71×10^{-6}	2.60×10^{-8}
10^6	6.75×10^{-7}	2.60×10^{-8}
10^7	6.76×10^{-8}	2.60×10^{-8}
10^8	7.78×10^{-9}	2.39×10^{-8}

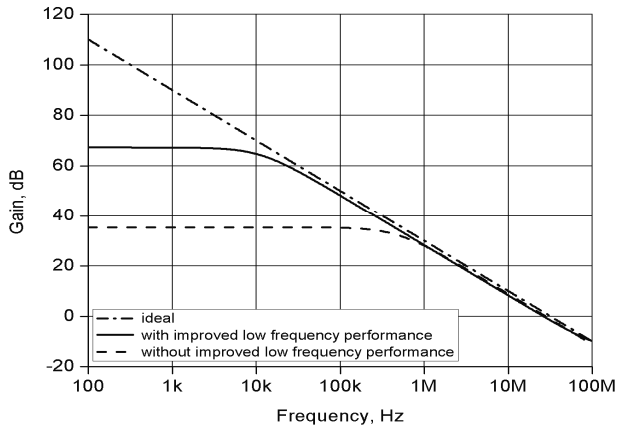

Fig. 8 — Frequency domain analysis of the ideal, proposed and simple integrator structures

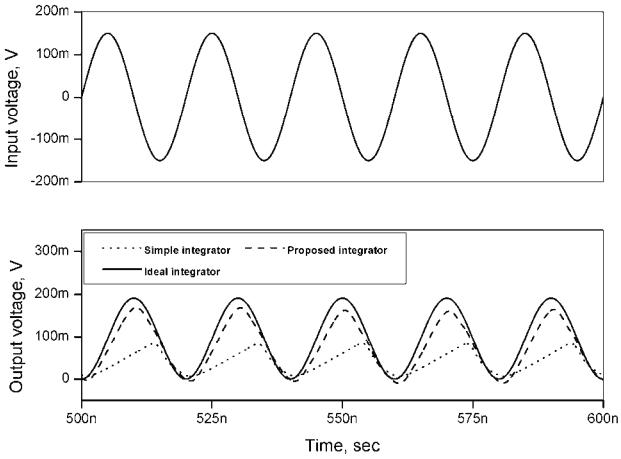

Fig. 9 — Time domain analysis of the ideal, proposed and simple integrator structures

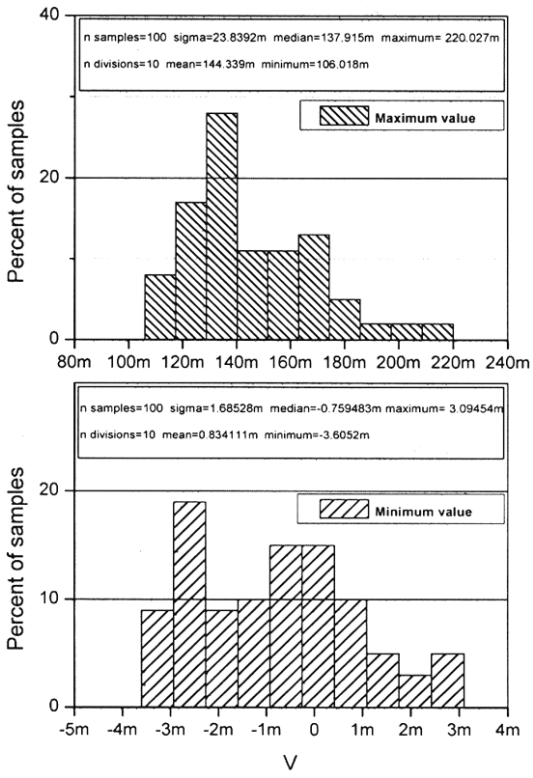

Fig. 10 — MC simulation result for the proposed integrator with 20% Gaussian deviation of the capacitor

In order to achieve experimental test, DDCC of the proposed IA can be constructed with four commercially available active devices[33] such as AD844s which can be easily replaced instead of the plus-type CCIIs (CCII+s) and five resistors as shown in Fig. 12. The passive components of the IA in Fig. 11 are selected as $R=R_1=R_2\cong 1k\Omega$. The applied input and corresponding output for the experimental test result are shown in Fig. 13.

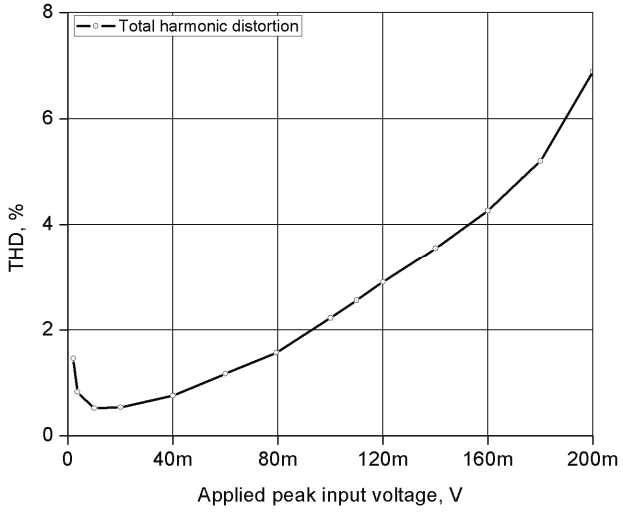

Fig. 11 — THD variations for the proposed integrator against peak values of sinusoidal voltage signal

It is observed from experimental result in Fig. 12 that the theory and experimental results agree quite well but the difference between them arises from parasitic impedances and frequency dependent non-ideal gains of the AD844s as well as parasitic of the board.

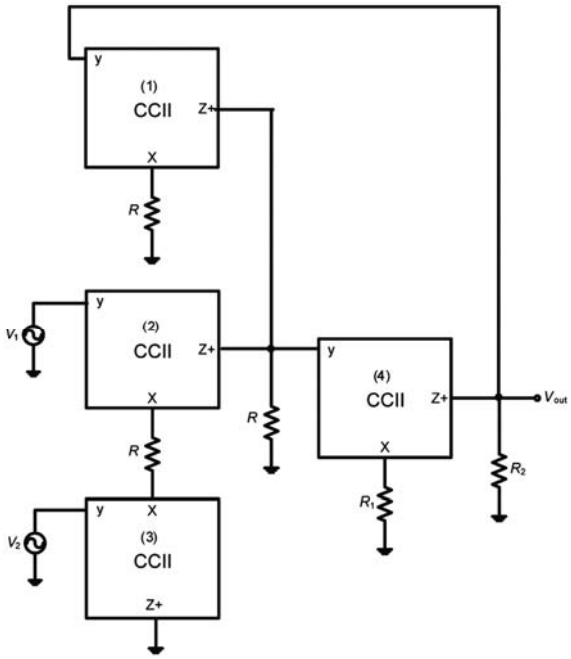

Fig. 12 — Realization of the proposed integrator with CCII+s to perform experiments

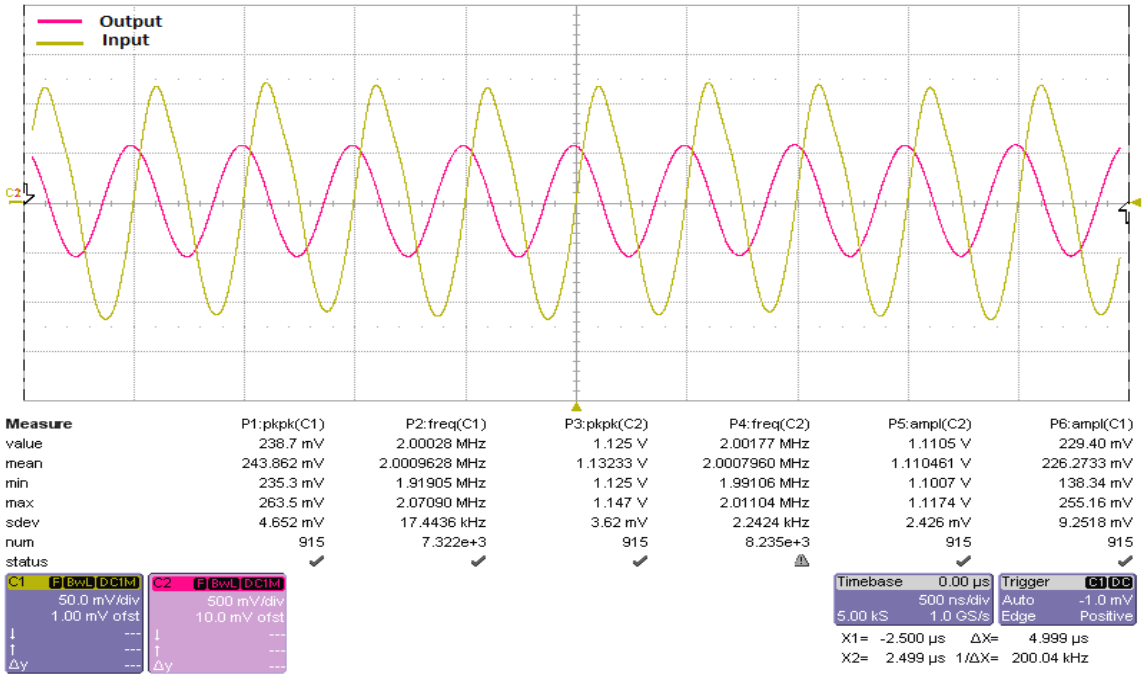

Fig. 13 — Experimental input voltage and corresponding output voltage for the proposed IA

5 Conclusions

In the present paper, very simple VM IA and integrator configurations containing only grounded passive components which are suitable for IC fabrication are developed. The proposed IA and integrator employ single DDCC. The proposed IA without needing critical passive component matching constraints can be constructed with only two small-valued resistors to obtain high gain value. The proposed integrator circuit has the feature of improved low frequency performances, which can be accomplished through a resistive component matching constraint. Both of the proposed configurations consume less power, and can be worked at higher frequencies. Some included simulation and experimental results confirm the theory well as expected.

References

1 Chiu W, Liu S I, Tsao H W & Chen J J, *IEE Proceeding-Circuits Devices & Sys*, 143 (1996) 91.
2 Pal K, *J Microelectronics*, 20 (1989) 37.
3 Toumazou C & Lidgey F J, *Electronics Letters*, 25 (1989) 228.
4 Surakampontorn W, Riewruja V, Surawatpunya C & Yodladda S, *International J of Electronics*, 71 (1991) 511.
5 Yuce E, *J of Circuits Sys & Computers*, 19 (2010) 689.
6 Maheshwari S, *International J of Electronics*, 89 (2002) 889.
7 Wilson B, *Electronics Letters*, 25 (1989) 470.
8 Ghallab Y H, Badawy W, Kaler K V I S & Maundy B J A, *IEEE Trans on Instrumentation & Measurement*, 54 (2005) 1941.
9 Gift S J G, *IEEE Trans on Instrumentation & Measurement*, 50 (2001) 85.
10 Yuce E & Minaei S, *J of Microelectronics*, 41 (2010) 311.
11 Azhari S J & Fazlalipoor H, *IEEE Trans on Instrumentation & Measurement*, 49 (2000) 1272.
12 Khan A A, Alturaigi M A & Elela M, *IEEE Trans on Instrumentation & Measurement*, 44 (1995) 887.
13 Ercan H, Tekin S A & Alci M, *Turk J Elec Eng & Comp Sci*, 20 (2012) 547.
14 Hassan T M & Mahmoud S A, *International J of Electronics & Communi (AEU)*, 64 (2010) 47.
15 Worapishet A, Demosthenous A & Liu X, *IEEE Transactions on Circuits & Sys*, 58 (2011) 699.
16 Safari L & Minaei S, *Circuits Sys & Signal Processing*, (2012).
17 Minaei S, *IEEE MELECON*, Dubrovnik Croatia, (2004).
18 Moradzadeh H & Azhari S J, *IEICE Electronics Express*, 5 (2008) 1017.
19 Horng J-W, *Circuits Sys & Signal Processing*, 27 (2008) 553.
20 Maheshwari S, *IET Circuits Devices & Sys*, 1 (2007) 72.
21 Minaei S & Yuce E, *Circuits Sys & Signal Processing*, 29 (2010) 295.
22 Yuce E, Minaei S & Alpaslan H, *J of Circuits Sys & Computers*, 20 (2011) 447.
23 Arslanalp R, Yuce E & Tola A T, *IET Circuits Devices Sys*, 7 (2013).
24 Maundy B, Gift S & Aronhime P, *IET Circuits Devices Sys*, 2 (2008) 201.
25 Wang Z, *Electronics Letters*, 26 (1990) 951.
26 Yuce E & Minaei S, *International J of Circuit Theory & Appli*, 36 (2008) 161.
27 Yuce E, Tokat S, Minaei S & Cicekoglu O, *International J of Electronics & Communi (AEÜ)*, 61 (2007) 580.
28 Sedra A S & Smith K C, *Microelectronic circuits*, Sixth edition, Oxford University Press, New York, (2010).
29 Yuce E, *IEEE Trans on Instrumentation & Measurement*, 57 (2008) 1079.
30 Yuce E, *IEEE Transactions on Circuits & Sys*, 55 (2008) 264.
31 Bruun E, *International J of Electronics*, 78 (1995) 911.
32 http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ibm-013/t97f_8hp_5lm-params.txt
33 Analog Devices 60MHz, 2000V/microsec Monolithic Op-amp, AD844.