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Study of parametric variations on hetero-junction vertical t-shape TFET for suppressing ambipolar conduction

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This paper investigates a hetero-junction vertical t-shape tunnel field effect transistor and discussed various methods for the suppression of ambipolar conduction for the first-time utilizing computer aided design sentaurus simulation tool. This device is primarily consisting of dual gate silicon based gated p-i-n diode for eminent control over the channel. Further, introduction to the 10 nm silicon germanium layer to the channel makes aggressive improvement to the device characteristics. Unlike to the conventional TFET, we have considered the effective techniques like gate-on-drain overlapping, gate-on-channel underlapping and different drain doping concentration up to 1×10^{18} cm^{-3}, which are used to conquer the ambipolar conduction by increasing the tunneling barrier width at the drain channel edges. The device surface potential performance is also analyzed for different parameters like drain doping concentration, gate-source voltage, silicon germanium $Si_{1-x}Ge_x$ mole fraction x and gate oxide thickness. Moreover, the vertical and lateral electric field inspect for determining the tunneling rate. The path distribution of source channel and drain in vertical direction will increase the scalability of the simulated device.

Keywords: Threshold voltage (V_T), Band-2-band tunneling (B2BT), SCEs (short channel effects), Subthreshold slope (SS), Vertical t-shape tunnel-FET (V-tTFET)

1 Introduction

The primary challenge of the complementary metal oxide semiconductor CMOS device with the continuous downscaling is to ensure consistency in the device's power consumption efficiency. However, working in the nano-scale regime along with reduced threshold voltage (V_T) will persuade to the several problems like mobility degradation, hot carrier effect (HCE), drain induced barrier lowering (DIBL) etc. It also restricts the physical capacity of thermally distributed carriers with a limited subthreshold slope at room temperature to 60mV/decade[1-3]. To address these issues, alternative transistor was evaluated using the band-2-band tunneling method technique to achieve lower subthreshold slope (SS < 60 mV/decade) at room temperature relative to the MOSFET. TFET has been found as a best alternative in respect to follow up the standards of the CMOS devices for low power consumptions[4-8]. Due to gate-controlled band-2-band tunneling (B2BT), TFET device is being investigated aggressively to acquire the subthreshold slope (SS) less than 60 mV/decade and endures the reduction in short channel effects (SCEs) comparatively with the conventional devices of MOSFET[9-10]. As the tunneling mechanism is occurred in the narrow channel region, TFET offers very less threshold voltage (V_T) and also reduce the leakage current in the series of Femto amperes (fA) at off state condition[4].

The systems will be more flexible in the era of TFET devices if the propagation path of the drain-source and channel approaches in the vertical direction[11,20]. Since the tunneling system allows a low energy band gap to keep the device efficient in terms of low V_{dd}, a high I_{on}/I_{off} current ratio, low threshold voltage (V_T) and steeper subthreshold slope (SS)[12,13]. This system involves measurements of the $Si_{1-x}Ge_x$ composition surface in the source-channel interface with specific mole fraction (x) with a low energy band gap of up to 0.7eV, resulting in a significant improvement in the gate-controlled tunneling probability compared to the silicon regulated devices[14,15]. But it additionally joins its unique property of ambipolarity, which need to be suppressed as it makes the device less suitable and effective for the complementary circuit design for low power digital circuit application[8]. Various methods have already been introduced to control the ambipolar conduction like heterogeneous gate dielectrics and large band gap hetero-junction material used in

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between drain channel interface to raise the depletion region thickness on the drain adjacent[16-18]. Despite the fact that the above strategies decrease the ambipolar transmission, they can prompt (a) reduction of ON-state current (b) increment in the drain series resistance and (c) included complexity in the process[19-21]. So, this paper turns out with various techniques like gate-on-drain overlapping, gate-on-channel underlapping and different doping concentration which are used to inhibit ambipolar actions of the device. Up to 1×10^{18} cm^{-3}, the doping concentration of drain will demonstrate the compelling command over the ambipolar current as discussed in the resulting outcomes. Now the surface potential is also examined and explored with adequate parameters like drain doping concentration, gate-source voltage, silicon germanium $Si_{(1-x)}Ge_x$ mole fraction x and gate oxide thickness (t_{ox}). Additionally, lateral (E_x) and vertical electric field (E_y) studied for various gate source voltage which can utilize for ascertaining the tunneling generation rate distribution for accomplishing drive current of the device.

2 Device Parameters and Simulation Models

A Vertical t-shape tunnel-FET (V-tTFET) consists of the source, channel and drain which are made up of silicon material with 10 nm silicon-germanium layer introduced into the channel to enhance the input characteristics. Source and drain length of the device is 30 nm each, while the channel length (L_g) is taken to be 60 nm. Figure 1 revealed the schematic diagram of TCAD simulated device of V-t TFET which consist of HfO_2 as an oxide material of 2 nm thickness with gate metal work-function of 4.15 eV.

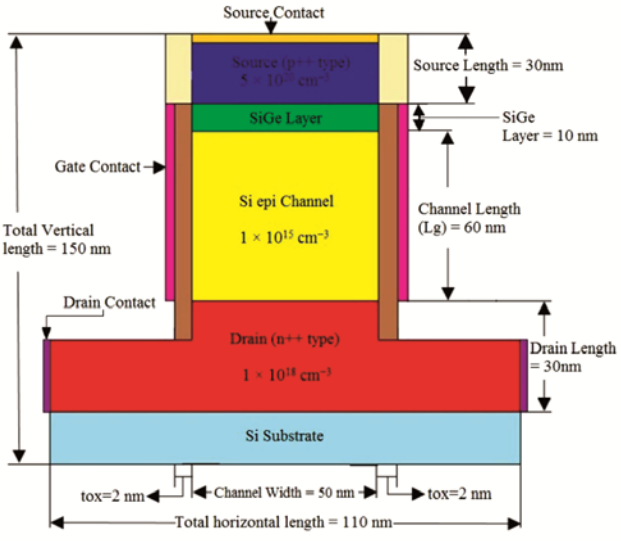

Fig. 1 – Schematic diagram of Vertical t-shape tunnel-FET (V-tTFET) with an embedded $Si_{1-x}Ge_x$ layer between source and channel.

Figure 2 refers to the conventional silicon material of vertical TFET structure calibrated at V_{ds} = 1 V with the drain characteristics curve.

Silicon material built device structure includes (*p++ type*) of 5×10^{20} cm^{-3} source doping concentration, (*n+ type*) of 1×10^{15} cm^{-3} doping concentration of channel and (*n++ type*) of 1×10^{18} cm^{-3} drain doping concentration as shown in Table 1. The device channel length is 60 nm with a 10 nm thin layer of $Si_{1-x}Ge_x$ among the source-channel interface. However, x is the mole fraction in $Si_{1-x}Ge_x$, which increases the germanium fraction by increasing the value of x. The pursuit of SiGe layer is due to lower band-gap 0.7eV of Ge material as connected to 1.1 eV of silicon material which will reduce the band gap between valance and conduction band to boost up the band-2-band tunneling (B2BT) in the direction to enhance drive current[22-24]. As SiGe sheet is integrated with the channel due to which the doping concentration of the silicon-germanium layer is same as that of channel. Moreover, if the whole channel is

Table 1 – Used device parameter for simulation.

Parameters	Values
Channel length (L_g)	60 nm
SiGe layer Thickness	10 nm
Channel Doping Concentration (*n+*)	1×10^{15} cm^{-3}
Source Doping concentration (*p++*)	5×10^{20} cm^{-3}
Drain doping Concentration (*n++*)	1×10^{18} cm^{-3}
Gate oxide thickness (t_{ox})	2 nm
Gate work-function (ϕ_m)	4.15 eV

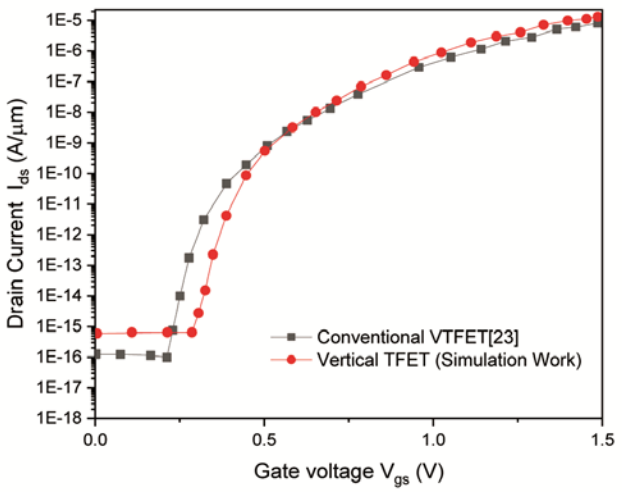

Fig. 2 – Calibrated drain current characteristics of vertical TFET compared with that of the corresponding conventional vertical TFET.

substituted by Ge/SiGe material or solitary a thin layer is provided on edge of the tunneling, both will have the same effect on the input characteristics[17]. Initially, due to increase in the OFF-state current, the percentage of drain doping concentration relative to the origin is kept low[18]. This occurs because of narrowing in the source epitaxial layer.

The energy band diagram shown in Fig. 3 (a) and Fig. 3 (b) has plainly been demonstrated the distinction between the silicon material n-type V-tTFET with presenting SiGe layer. The p-i-n structure energy band diagram of $Si_{(1-x)}Ge_x$ 10 nm layer is driven with x = 0 and 0.8 mole fraction which makes the tunneling path narrower for B2BT as shown in Fig. 3 (b). Now for reduction of the ambipolar current various approaches have been discussed. Unlike to the

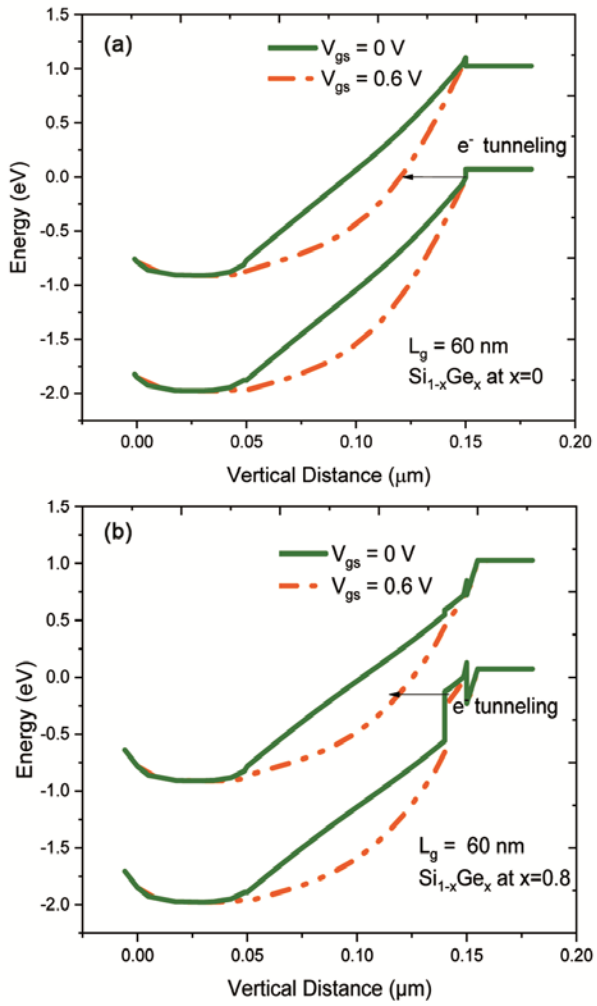

Fig. 3 – (a) Simulated energy band diagram for the Silicon Vertical t-shape Tunnel FET as a function of V_{gs} = 0 V & 0.6 V at V_{ds} = 0.5 V and (b) simulated band diagram for introduced SiGe layer (x=0.8) Vertical t-shape Tunnel FET as a function of Vgs = 0 V & 0.6 V at Vds = 0.5 V.

conventional TFET, where gate terminal controls only channel region. However, in the proposed device, the gate-on-drain overlapping and gate-on-channel underlapping with a variation of drain doping concentration are discussed in result analysis along with surface potential variation for different parameters. TCAD sentaurus 2D simulation of the device is performed using B2BT non-local path framework[25-27]. By using a non-local phonon-assisted band-2-band tunneling, the complete tunneling potential pathway is traced[8]. This model comprises the phonon-assisted tunneling process which is important for indirect band gap materials, as well as strain effects present at the interface between the Si and the SiGe layers that can modify the band structure of the material. In addition, the mobility model of the Lombardi and Standard Shockley-Read-Hall (SRH) recombination are also cast for simulation work[15,24].

3 Results and Discussion

3.1 Vertical t-TFET (n-type) with gate-on-channel undelapping condition for ambipolar reduction

In this caption, we have demonstrated various methods to overwhelm the ambipolar conduction, which is one of the integral properties of the vertical t-shape Tunnel FET. In conventional TFET, the polarity of gate depends on source-channel and the drain-channel tunneling barrier. As we apply the positive (+) gate voltage to the device, the source-channel interface tunneling barrier will become narrower which causes to increases in the drain current. However, if the gate voltage polarity becomes negative (-) then it will narrow the drain-channel barrier which lead to rise in ambipolar current. This makes the device inadmissible for the complementary functions of the digital circuits. To restrain the ambipolar current, the interface of channel and the drain should not be narrowed. Three methods were testified and are discussed to conquer the ambipolar conduction of the V-tTFET device through simulation. First one is to introduce with the underlap condition in which only half of the channel is surrounded by the gate terminal form both sides. In the second case the gate terminal is overlapping in the drain terminal, whereas the third consist of the dipping the drain doping concentration. As clearly shown a description of Fig. 4 and Fig. 5 regarding the underlap and overlap condition of the gate terminal which contribute a major role in suppressing the device's ambipolar current.

Figure 4 shows the underlap region of the channel without any gate terminal contact over it. The distance between the gate terminal and drain region introduces the underlap region between them due to which the resistance between the channel drain barrier increases. This causes to increase in tunneling distance at gate-drain region and decreases the unwanted ambipolar conduction. It is depicted from Fig. 5 that with the reduction of 5 nm gate terminal of the drain side, the ambipolar current will start decreasing and reached up to the 10^{-17} A/μm at V_{ds} = 1 V.

3.2 Vertical t-TFET (n-type) with gate-on-drain overlapping condition for ambipolar reduction

Figure 6 shows the schematic diagram of a second case gate-on-drain overlapping condition. Unlikely to the conventional TFET where source-channel interface and drain-channel interface are controlled by a gate terminal for different polarity. However, in the proposed device, the gate-on-drain overlapping will limit the tunneling current control only at the source-channel edge irrespective to the gate terminal division. Since gate terminal will surround the drain region, the applied voltage in the gate terminal will be uniform in the channel and gate-on-drain overlapped region. As a result, even in the negative gate voltage, the *n*+ drain-channel interface tunneling barrier will not be further depleted. It will reduce the overall conduction to the ambipolarity of the device.

It is described from Fig. 7 that with the negative polarity at gate-terminal overlap on the drain surface determines the control over the ambipolar current. The overlap length is increase with the variation of the 2 nm each as shown in the figure. So, therefore gate-on-drain overlapping method does not only

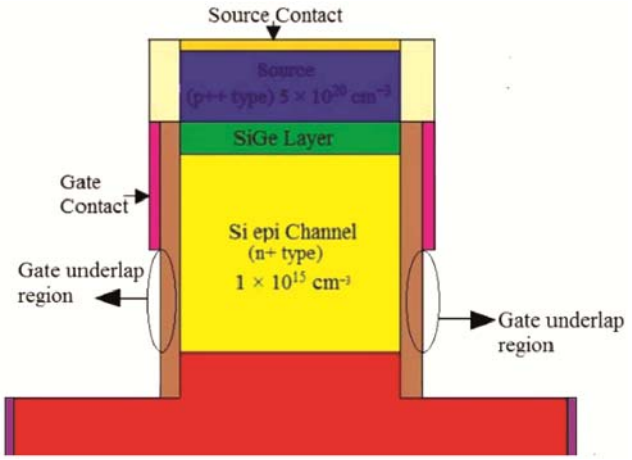

Fig. 4 – Schematic structure of gate-on-channel underlapping vertical t-shape tunnel FET.

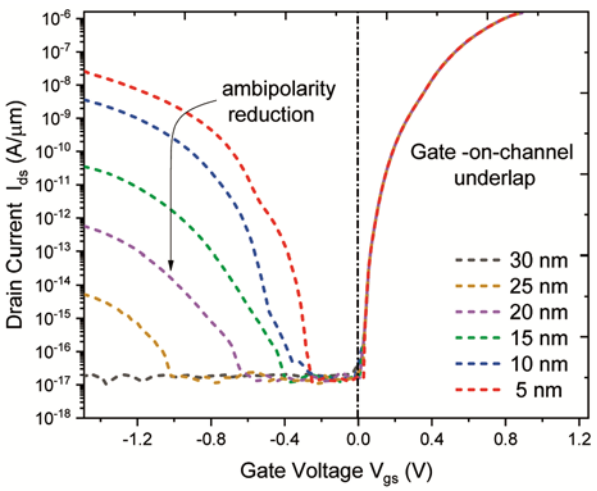

Fig. 5 – Transfer characteristics of gate-on-drain underlapping vertical t-shape tunnel FET.

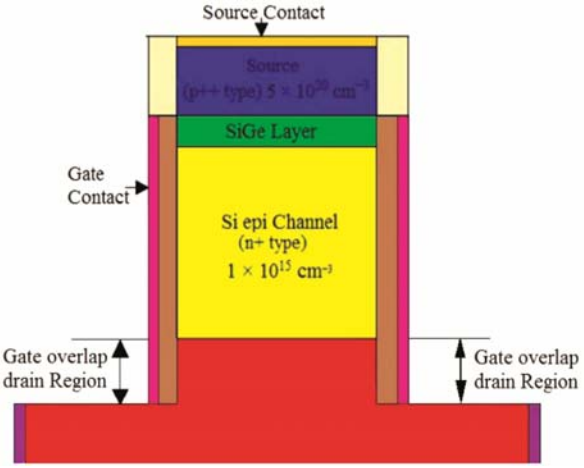

Fig. 6 – Schematic structure of the gate-on-drain overlapping vertical t-shape tunnel FET.

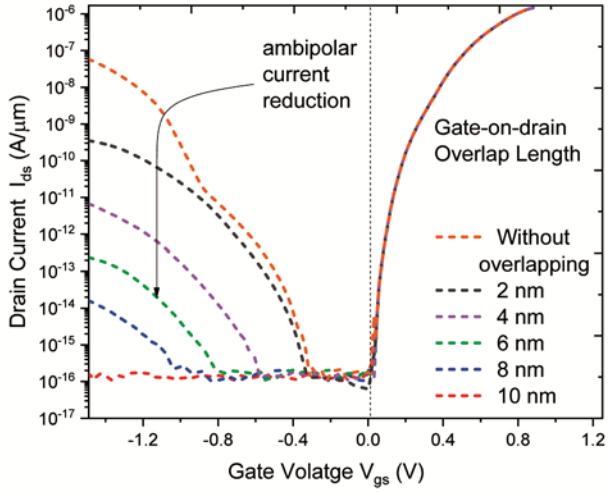

Fig. 7 – Transfer characteristics of the gate-on-drain overlapping vertical t-shape tunnel FET.

suppress the ambipolar current but also kept the capacitance to its minimum value.

3.3 Vertical t-TFET (n-type) with the effect of drain doping concentration for ambipolar reduction

Now, in third case, a drain doping concentration variation is being discussed in order to reduce the ambipolar current. Figure 8 shows the ambipolar current decreases propotionally with the drain doping concentration in projected device.

Figure 9 shows the energy band diagram corresponding to the variation in drain doping concentration from 1×10^{18} to 1×10^{20} cm^{-3} at V_{gs} = 0.6 V and V_{ds} = 0.5 V with the device's channel length of 60 nm. The tunneling barrier diameter becomes wider up to the range of 10^{18} cm^{-3}, but as the drain doping concentration increases up to the range of 10^{20} cm^{-3}, the gate potential at the drain overlap area becomes insufficient to modulate the band narrowing. Therefore, it will result in the narrowing tunneling barrier with a rise in the ambipolarity. However, if drain-doping concentration increases up to 1×10^{20} cm^{-3} the tunneling barrier will begin narrowing and it will prompt to increase in the device current towards the drain side even in the negative gate polarity results to an ambipolar conduction. With above analysis we kept optimized value for drain doping concentration as 1×10^{18} cm^{-3}.

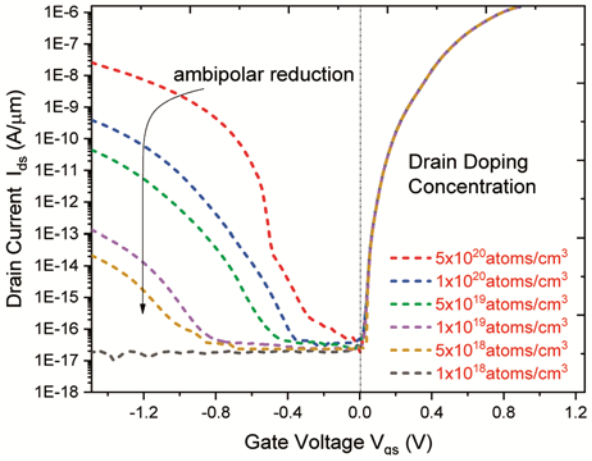

Fig. 8 – Transfer characteristics of V-tTFET device on drain doping concentration.

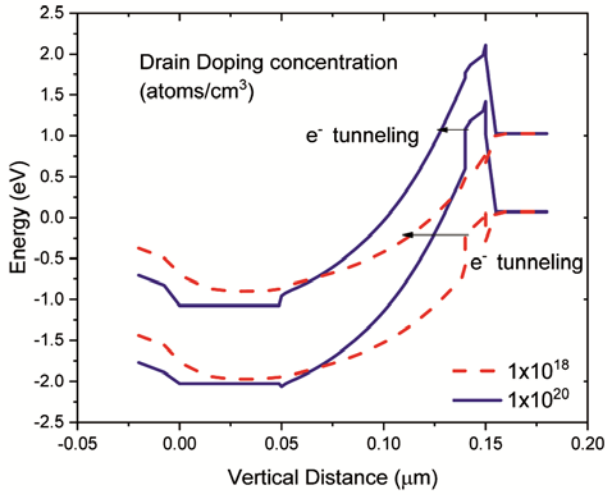

Fig. 9 – Simulated band diagram of drain doping concentration of vertical t-shape tunnel FET varying from 1×10^{18} to 1×10^{20} cm^{-3} as a function of V_{gs} = 0.6 V at V_{ds} = 0.5 V.

3.4 Effect of drain doping concentration on surface potential

Now electrical characteristics of the device simulated through TCAD as a function of drain doping concentration, channel length (L_g), oxide thickness (t_{ox}) and Silicon-Germanium mole fraction variation are discussed as a function of surface potential. The device's channel potential at the silicon-oxide interface is defined as the surface potential. Figure 10 shows the impact of doping concentration variation on the surface potential in between the channel of the device ranging from 5×10^{17} cm^{-3} to 1×10^{20} cm^{-3}. The figure shows that the surface potential increases proportionally with increase in drain doping concentration as upsurges of the charge carrier.

3.5 Effect of gate-source voltage on surface potential

The determined surface potential profile for the different gate biasing voltage (V_{gs}) ranging from 0.55 to 0.80 V of the vertical t-shape tunnel FET is discussed in Fig. 11. It can be observed from the figure that the surface potential in the lightly doped area i.e.

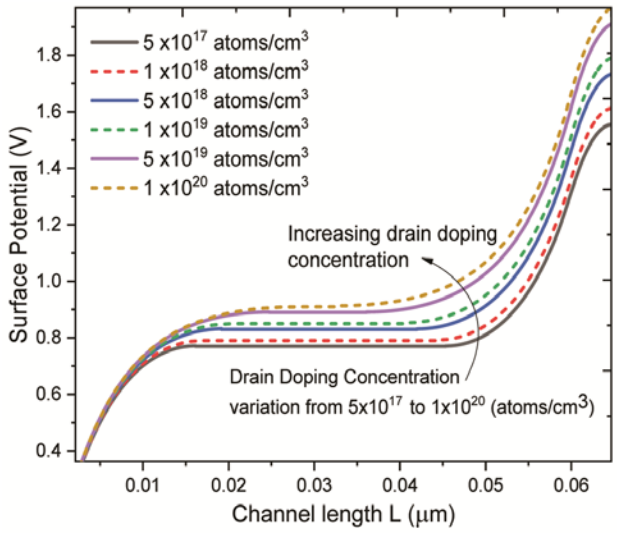

Fig. 10 – Surface potential variation in between the channel due to drain doping variation.

channel, will also increase proportionate to the gate-source voltage (V_{gs}). Increasing in gate-source voltage, leads to an increase in capacitance which also improves the band-2-band tunneling rate. From the figure, it is clearly observed that the surface potential will initially high at the drain-channel interface region as compared to the source-channel interface. This happens due to the great influenced of the drain biasing over the entire channel.

3.6 Effect of silicon-germanium mole fraction on surface potential

Now in Fig. 12, the surface potential is analyzed with the mole fraction variation of silicon germanium $Si_{(1-x)}Ge_x$ ranging from 0.4 to 0.8. From the figure it is depicted that with the rise in the mole-fraction of the silicon germanium the energy band gap start reduces from 1.1 eV to 0.7 eV which leads to the increase in B2BT rate and on-state current along with the surface potential at source-channel junction.

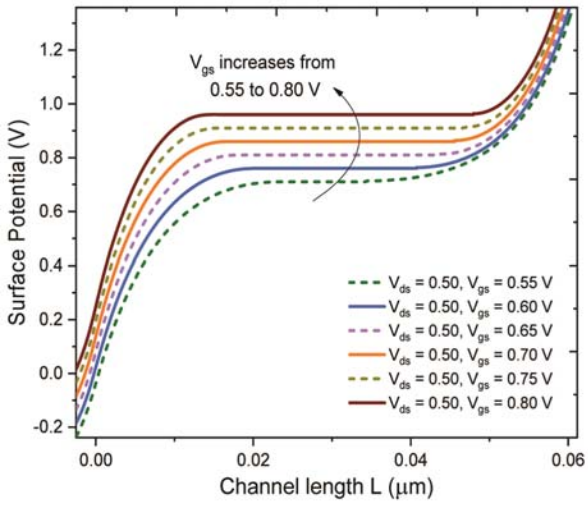

Fig. 11 – Variation of the surface potential with V_{gs} for channel length L_g = 60 nm at V_{ds} = 0.50 V of the device V-tTFET .

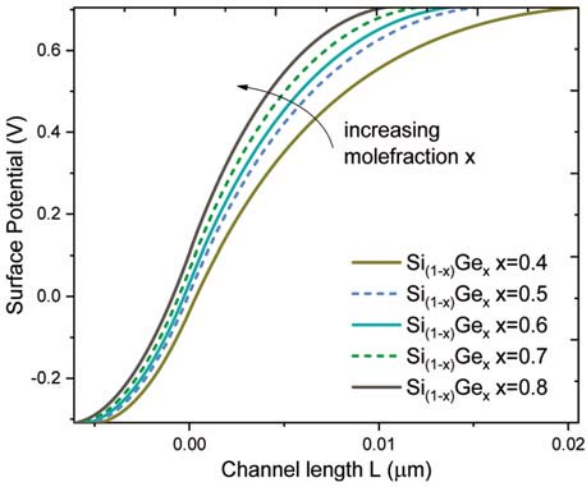

Fig. 12 – Surface potential profile with a variation of silicon germanium $Si_{(1-x)}Ge_x$ mole fraction x for channel length L_g = 60 nm at V_{ds} = 0.5 V.

3.7 Effect of gate oxide thickness on surface potential

Figure 13 indicates the surface potential transfer characteristics with relative to oxide thickness variance from 5 nm to 2 nm. It is observed and evaluated from the figure that the capacitance across the device will rise with the reduction of oxide thickness (t_{ox}), contributing to the strong ON-state current along with the surface potential.

3.8 Effect of gate-source voltage on vertical electric field on device

Figure 14 displays the simulated values of the vertical electrical field (E_Y) as a function of gate

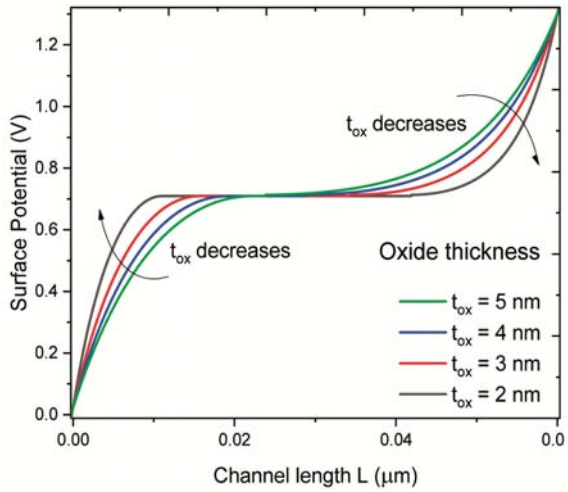

Fig. 13 – Surface potential profile with the variation in the oxide thickness (t_{ox}) of the device channel length L_g = 60 nm at V_{ds} = 0.5 V.

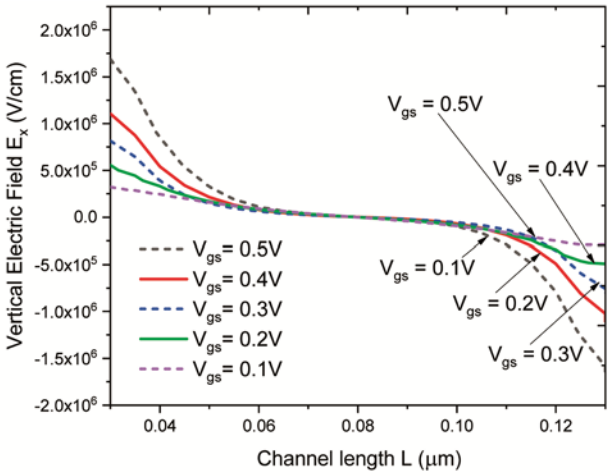

Fig. 14 – Vertical electric field E_Y of Vt-TFET for different V_{gs} at V_{ds} = 1 V with channel length L_g = 60 nm.

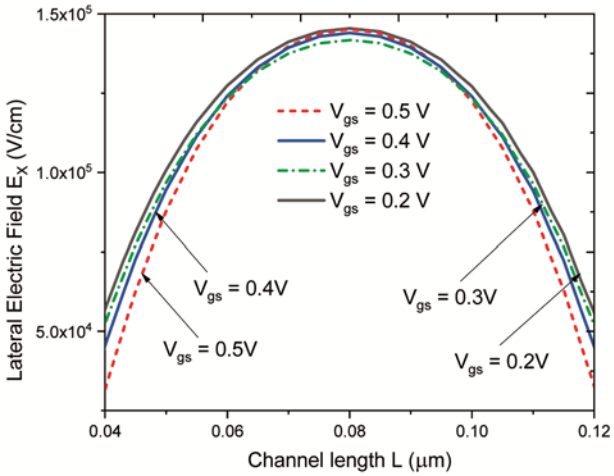

Fig. 15 – Different V_{gs} analysis for lateral electric field E_x of Vt-TFET for channel length L_g = 60 nm at V_{ds} = 1 V.

voltages (V_{gs}) in the device. The maximum variation of the vertical electrical field appears nearer to the source side, contributing to the raise in the tunneling generation rate. Therefore, the tunneling current will increase and have much more effect of the vertical electric field as compared to that of the lateral electric field.

3.9 Effect of gate-source voltage on lateral electric field on device

In Fig. 15, the device is tested for 60 nm channel length with respect to lateral electric filed E_x as a function of different gate voltage. The drain-source (V_{ds}) voltage will basically contribute the lateral-electric field E_x, this turns into the decrease of gate control over the channel[28]. The figure shows that the lateral electrical field E_x across the middle of channel will remain almost constant for various gate voltages relative to the source and drain junction. The potential variation is restricted to a small area of the tunneling junction with the effect of biasing voltage V_{gs} as compared to that of vertical electric field (E_Y). Clearly, the diagram results in the lateral electrical field being less prevalent on the device as compare to the vertical electrical field.

4 Conclusions

Vertical t-shape tunnel FET was investigated and analyzed in this paper for the improvement its performance over the various parameters. Using sentaurus TCAD simulations, we have studied effective methods like gate-on-drain overlapping, gate-on-channel underlapping and with the different doping concentration which are used to eliminate the device's ambipolar current. Up to the value of 1×10^{18} cm^{-3} of drain doping concentration, it will show effective control over the ambipolar current. Now the effective parameter like drain doping concentration, gate-source voltage, silicon germanium $Si_{(1-x)}Ge_x$ mole fraction x and gate oxide thickness which influence the surface potential are also analyzed and investigated. Further the lateral and the vertical electric field studied for different gate source voltage which can used for calculating the tunneling generation rate distribution for achieving drive current of the device. So, the results clearly reflect that the device immunity against the ambipolar conduction with reduced leakage current and improved drive current. Nevertheless, there is still room remaining to expand the functionality of the device with an adequate selection of the gate work-function and use of the dual gate terminal. Vertical t-shape tunnel FET is therefore considered to be a promising candidate for electronic applications with low power and ideal for future technology.

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