# Optimized multiplexer design and simulation using quantum dot-cellular automata

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Recent trends in nano technological field are the exploitation of quantum dot-cellular automata (QCA) as a substitute in advance to existing transistor based CMOS technology to fabricate nano-circuit. Ultra low heat dissipation, faster clocking and high device density make the QCA as a raising research area in nanotechnological field to suppress the FET based circuit. This paper illustrates a simple and basic method to design QCA based 2:1 multiplexer at nanoscale. The proposed 2:1 multiplexer is compared with the previously designed 2:1 multiplexer in account of circuit density, clock zone numbers, amount of QCA cell used to design the circuit and the density consumed by all QCA cell over total density of the circuit is depicted. This comparative analysis has approved the efficiency of the proposed design. The circuit is implemented and proved using QCA designer-2.0.3.

Keywords: QCA, Clocking, Majority gate, Multiplexer

## 1 Introduction

In recent era, QCA provides a new novel nanotechnological model of computing that may be an alternative way out to CMOS circuit[1,2]. In QCA operation, information is encoded based on electron's charge configuration within a QCA cell of coupled quantum dots[3-8]. Due to cells mutual columbic interaction with each other, all the cells reveal bi-stable behavior that is sufficient to perform the computation, and binary information can be encoded; no current flows happened out of cell. This is a remarkable break with the currently used transistor based model (CMOS). CMOS circuit possesses multiple problems related to the timing of operations as because it's different component are highly coupled with each other and many physical limits also exist[9-17]. According to Moore's law the number of chips implanted in a single device will raise in every 1 year 6 months and as a consequence of it the circuit's complexity will increase. This will led to difficulty in synchronization. Due to some physical phenomenon it will be an immense issue for future scalability of CMOS circuit. So a transistor less technology is necessitated and QCA does this. In QCA power consumption is very low; it has high density and also possesses high clocking frequency[18-20]. The recent trend in circuit design is to minimize the complexity

of integrated circuit, i.e., increased circuit density and in that context QCA may be handy. In QCA messages are propagated by using the electronic induction effect which comes into effect due to the presence of electrons within the quantum dots instead of electrical pulse like in CMOS circuit[21-24]. This paper illustrates a simple and basic technique to design 2:1 multiplexer using QCA. The improvement of proposed design in terms of circuit density, number of clock zones, number of QCA cell used and area usages by proposed 2:1 multiplexer over previously designed 2:1 multiplexer is described. QCA Designer-2.0.3[25] is employed to implement and test the circuits.

In digital data transmission at nanoscale, the hardware complication in terms of power consumption and circuit density for signal encoding are challenging concern. This work has the contributions as follows:

(i) An optimized 2-to-1 multiplexer design using QCA at nanometer scale.

(ii) A detailed comparative study with the previously designed 2:1 multiplexer on account of circuit's density, number of clock zones, number of QCA cell is achieved.

(iii) The simulation result is analyzed with the theoretical values fixed the computational functionality of the proposed design.

A QCA cell is a charge container of four quantum dots[26-30] which are covered by insulating substance.

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Each dot is linked through a metallic tunneling line via which the electron can traversed from dot to dot as shown in Fig.1(a). First of all two free extra electrons are embedded into a QCA cell. Due to repulsive force of electrons, they are placed at the corner position of the QCA cell called cell's polarization symbolized by $P$ exposed in Fig. 1(b). In a QCA cell can clasped binary '1' and '0' if $P=+1$ and $P=-1$, respectively. $P=0$ points out an un-polarized cell, i.e., holds no information[30-34].The primary gate used in QCA circuit is majority gate having three inputs shown in Fig. 2(a) and corresponding QCA arrangement is shown in Fig. 2(b). The truth table is shown in Table 1. Output of majority gate is calculated inputs majority[35-38]. Let $P$, $Q$ and $R$ be the majority gate inputs and then majority logic expression can be written as:

$$M (P, Q, R) = PQ+ QR+RP \qquad ...(1)$$

If one of $P$, $Q$, $R$ is fixed to '0' or '1', the logic and function and or function can be carried out as in Fig. 3(a) and Fig. 3(b), respectively[39-42] and written as:

$$M (P, Q, 0) = P.Q \qquad ...(2)$$

$$M (P, Q, 1) = P + Q \qquad ...(3)$$



Binary '0'    Binary '1'    Null

Electron
Quantom
Dot
$P=-1$    $P=+1$    $P=0$
(a)       (b)       (c)
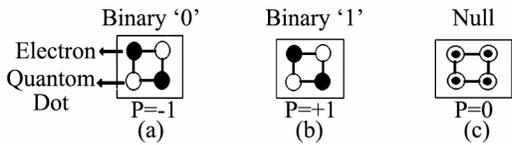
Fig. 1 – QCA cell polarization



(a)                (b)
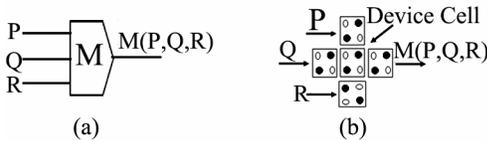
Fig. 2 – Majotrity gate's (a) QCA schematic and (b) QCA layout

Table 1 – Truth table of majority gate

| | Input | | Output |
|---|---|---|---|
| $P$ | $Q$ | $R$ | $M(P,Q,R)$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

If QCA cells are arranged in consecutive manner then QCA wire is formed. The mutual electrostatic interaction between cells caused propagation of information through wire as in Fig. 4. Mainly, 90° wire and 45° wire[19,28] are present. This is shown in Fig. 4(a) and Fig. 4(b), respectively. The polarization of all cells in 90° wire remains same whereas in 45° wire alternates in each consecutive cell of the wire[43-45].When QCA cells are at corners touching position (at 45° angle) with each other then QCA NOT-gate (inverter) is formed as in Fig. 5[6,21-22]. The electrostatic repulsion of cells caused the conversion of logic value '0' and '1' into '1' and '0', respectively. In QCA, the adiabatic switching mechanism is present[19-21]. The switching is occurred in four clocking zones. Each zone is lagged by $\pi/2$[12-14] as shown in Fig. 6. This helps to design circuit at nano scale in diverse mode than CMOS circuits. Switch phase- in this phase the polarization of QCA cell is started. The electron starts switch between dots.



(a)                (b)
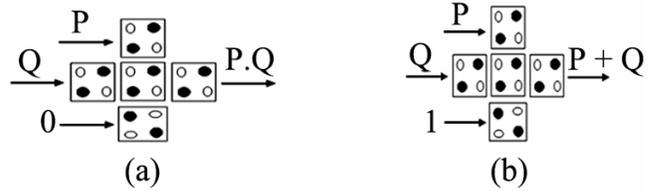
Fig. 3 – (a) QCA AND- gate and (b) QCA OR- gate



Flow of Information          Flow of Information

(a)                (b)
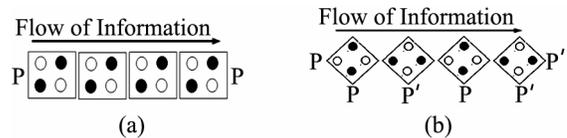
Fig. 4 –QCA (a) 90° wire and (b) 45° wire



(a)                (b)
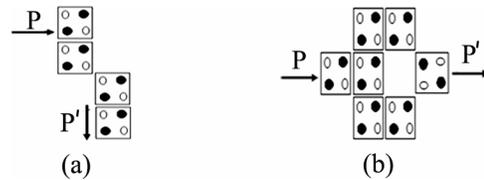
Fig. 5 – QCA inverters



(a)                (b)
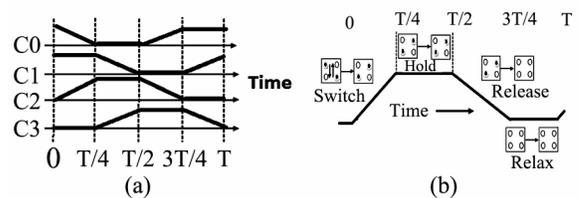
Fig. 6 – (a) Clocking phases and (b) QCA operation at the time of one clock phase

Hold phase- the previously achieved cell polarization remain same. The barrier between dots is in high condition. The electron can't tunnel. Release phase-QCA cell starts to loss its polarization. The barrier between dots is lower. The electrons can able to tunnel through dots. Relax phase-barrier remains at lower state. The cell becomes un-polarized[22-23].

## 2 Proposed Multiplexer Design Using QCA

### 2.1 Multiplexer

A Multiplexer[26-31] is a digital combinational circuit. Numerous data inputs are present, among them one or more are select inputs and one of them acts as output. Signal values are passed from one of the inputs to output. The select input required to select the data input as shown in Fig. 7.

### 2.2 Proposed 2-to-1 multiplexer

The 2-to-1 multiplexer[26-31] has two inputs as $W_0$ and $W_1$, one selection line as $S$ and one output line as $F$ exposed in Fig. 8. When selection input $S$ is '0' then output will be $W_0$ and when $S$ is '1' then output will be $W_1$ as shown in Table 2. Using truth
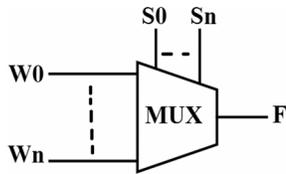


Fig. 7 – Graphical symbol of multiplexer
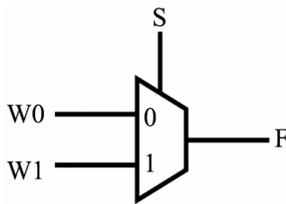


Fig. 8 – Graphical symbol of 2:1 MUX

Table 2 – Truth table of 2:1 MUX

| | Input | | Output |
|---|---|---|---|
| $S$ | $W_0$ | $W_1$ | $F$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Table 2 the logic expression for 2-to-1 MUX can be produced as:

$$F = W_0.S´ + W_1.S \qquad \ldots(4)$$

QCA majority gate expression for the proposed circuit is shown in Eq. 5:

$$F = M\,(M\,(W_0, S´, 0),\, M\,(W_1, S, 0),\, 1) \qquad \ldots(5)$$

The schematic and layout in QCA is shown in Fig. 9(a) and Fig. 9(b), respectively.

### 2.3 Previously designed 2-to-1 multiplexer

Various previously implemented 2:1 multiplexer using QCA, are taken into account and a more effective as well as effective design is depicted in this paper. The suggested 2:1 multiplexer circuit is compared with the previously designed multiplexer[27-29,31-38] depending on the number of clocking zones, as well as area and circuit's complexity. Figures 10-12 show the different formerly designed multiplexer circuits. The multiplexers[27, 29] require three layers; whereas the multiplexer presented in[29] is smaller in size as well as much more proficient than multiplexer explored in[28]. On the other hand the multiplexer[32] consumes less input to output delay than the multiplexer proposed[27-29,31]. The multiplexer presented in[33] has less cell count than multiplexer reported in[34-38] but the multiplexer[38] is similar to multiplexer presented in[32] and better than all other multiplexers[27-29,32-37] with respect to clocking zones used. Irrespective of multiplexer[33], the reported multiplexer in[39] has less number of cells and its device density is much higher compared to other existings[27-29,32,34-38].

## 3 Results and Discussion

Implementation and simulation of proposed design is achieved using QCA Designer-2.0.3[25]. Figure 13 shows the simulation result of 2:1 MUX. From Fig. 13, it can be seen that when $S$=0, then output is $W_0$, i.e., OUT=0 (if $W_0$=0) or OUT=1 (if $W_0$=1) and when $S$=1, then output is $W_1$, i.e., OUT=0 (if $W_1$=0) or OUT=1 (if $W_1$=1) and so on. All the circuits are verified with original truth table. The following list of parameters which are required for obtaining the bi-stable approximation: Each cell's height is 18 nm, its width 18 nm, dot diameter 5 nm, number of samples 12800, relative permittivity 12.900, maximum iterations in each sample 1000, clock low 3.80000e-23J, clock high 9.80000e-22J, clock amplitude factor 2.0000, radius of effect 65.00 nm, and convergence tolerance is 0.001000 and layer
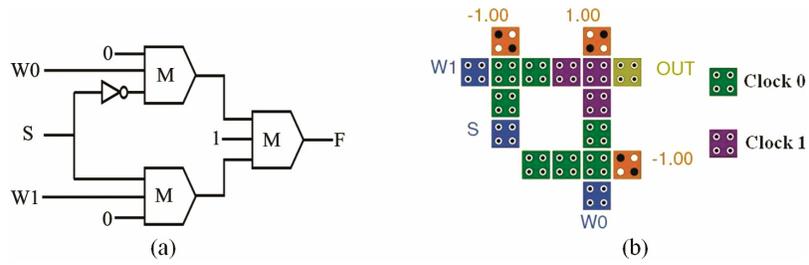
Fig. 9 – (a) Schematic of proposed 2:1 MUX and (b) QCA layout of proposed 2:1 MUX
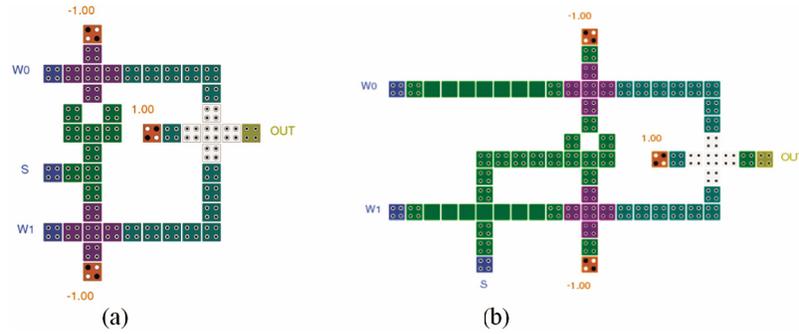


Fig. 10 – 2:1 MUX (a) existing[27] and (b) existing[28]
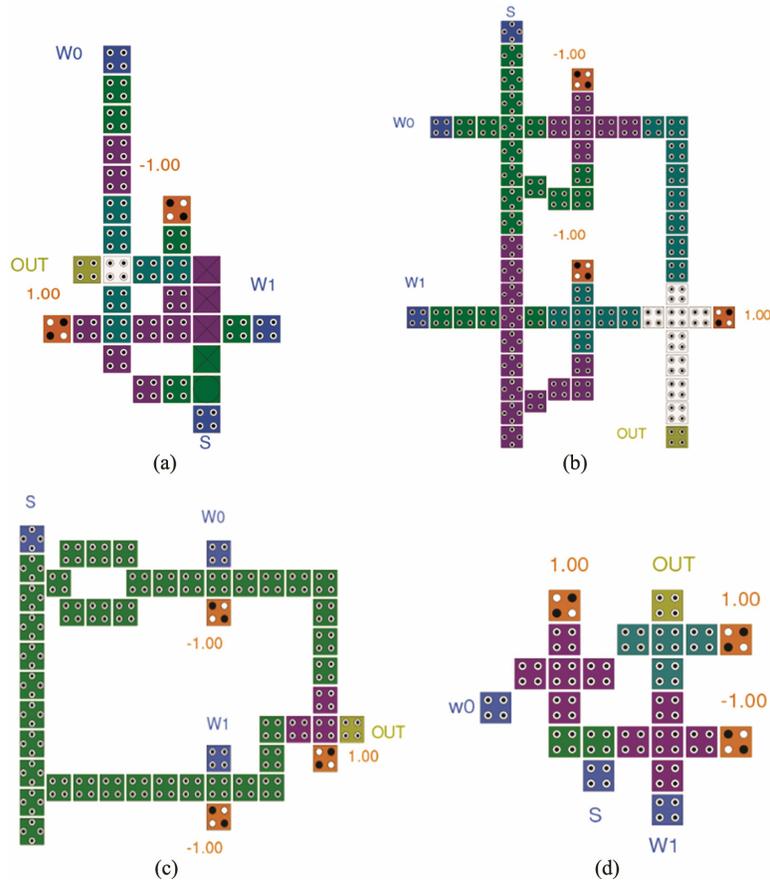


Fig. 11 – 2:1 MUX (a) existing[29], (b) existing[31], (c) existing[32] and (d) existing[33]
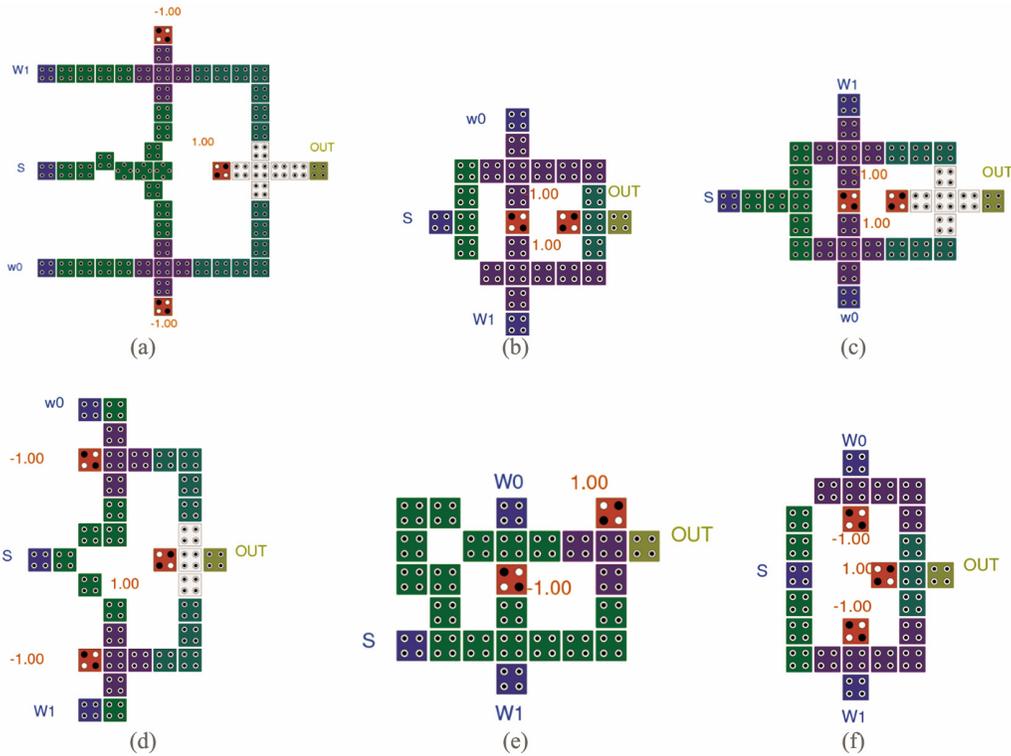
Fig. 12 – 2:1 MUX (a) existing[34], (b) existing[35], (c) existing[36], (d) existing[37], (e) existing[38] and (f) existing[39]
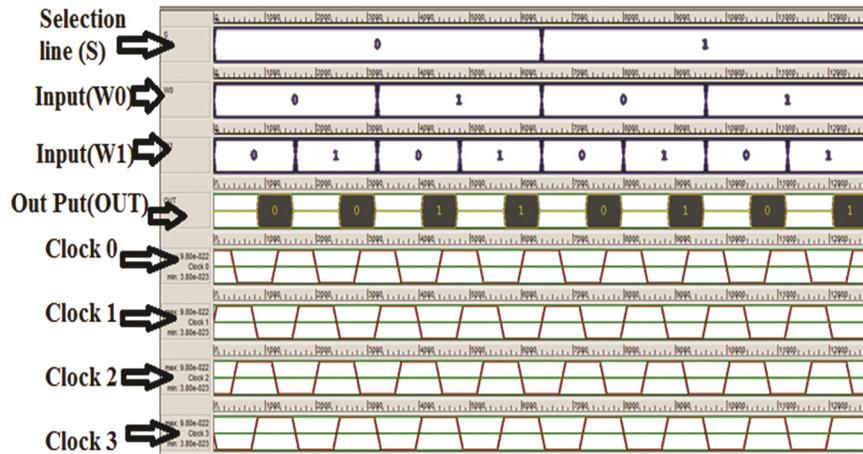


Fig. 13 – Simulation result of 2:1 MUX

separation is 11.50000 nm. Table 4 describes the detailed comparisons of proposed multiplexer with the previously designed multiplexer[27-29,31-38]. Figure 14 shows the number of QCA cell required by proposed design of 2:1 MUX and previous work whereas Fig. 16 shows the total area consumed by proposed 2:1 MUX and previous work. The cell area, area usages and number of clock zones used in proposed 2:1 MUX and previous design is displayedin Fig. 15, Fig. 17 and Fig. 18, respectively.

Percentage reduction of total area, cell area and area usage of proposed circuit over previous circuit is described in Fig. 20, Fig. 21 and Fig. 22, respectively. Figure 19 shows the improvement of stated circuit in form of percentage reduction of number of QCA cell required by proposed design of 2:1 MUX over previous circuit where as the improvement of stated circuit in terms of clocking zones used in proposed 2:1 MUX over previous design is depicted in Fig. 23.

Table 3 deals with the complexity of proposed circuit with respect to QCA cells, QCA inverters, majority gates, clocking zones and circuit area applied to design the circuit. From Table 3 clearly portrays that the proposed 2:1 MUX circuit requires 3 MVs, 1 inverter, 2 clock zones, 17 cells and 11664 nm² areas but usage area is only 47.22%. Detailed comparative study with the previously designed 2:1 multiplexer on account of circuit's density, number of clock zones, and number of QCA cell is explored in Table 4. The comparison shows that the proposed 2:1 multiplexer has less cell count and lower device area than that of existing multiplexers.

Table 3 – Circuit complexity

| Proposed QCA circuit | Number of majority gate used | No of QCA cell | Total area (nm$^2$) | Cell area (nm$^2$) | Area usage (%) | Clocking zones |
|---|---|---|---|---|---|---|
| 2:1 MUX | 3 majority gates and one inverters | 17 | 11664 | 5508 | 47.22 | 2 |

Table 4 – Circuit complexity

| Proposed QCA 2:1 MUX circuit | Number of majority gate used | No of QCA cell | Total area (nm$^2$) | Cell area (nm$^2$) | Area usage (%) | Clocking zones |
|---|---|---|---|---|---|---|
| Proposed | 3 majority gates and one inverter | 17 | 11664 | 5508 | 47.22 | 2 |
| Existing[27] | 3 majority gates and one inverter | 46 | 46332 | 14904 | 32.16 | 4 |
| Percentage reduction w.r.t[27] | | 63.04 | 74.82 | 63.04 | 15.06 | 50 |
| Existing[28] | 3 majority gates and one inverter | 75 | 99792 | 24300 | 24.35 | 4 |
| Percentage reduction w.r.t[28] | | 77.33 | 88.31 | 77.33 | 22.87 | 50 |
| Existing[29] | 3 majority gates and one inverter | 31 | 37908 | 10044 | 26.50 | 4 |
| Percentage Reduction w.r.t[29] | | 45.16 | 69.23 | 45.16 | 20.72 | 50 |
| Existing[31] | 3 majority gates and two inverters | 67 | 81648 | 21708 | 26.58 | 4 |
| Percentage reduction w.r.t[31] | | 74.63 | 85.71 | 74.63 | 20.64 | 50 |
| Existing[32] | 3 majority gates and one inverter | 49 | 46332 | 15876 | 34.26 | 2 |
| Percentage reduction w.r.t[32] | | 65.30 | 74.82 | 65.30 | 12.96 | 0 |
| Existing[33] | 3 majority gates and two inverters | 23 | 18144 | 7452 | 41.07 | 3 |
| Percentage reduction w.r.t[33] | | 26.08 | 35.71 | 26.08 | 6.15 | 33.33 |
| Existing[34] | 3 majority gates and one inverter | 57 | 72900 | 18468 | 25.33 | 4 |
| Percentage reduction w.r.t[34] | | 70.17 | 84 | 70.17 | 21.89 | 50 |
| Existing[35] | 3 majority gates and one inverter | 27 | 23328 | 8748 | 37.50 | 3 |
| Percentage Reduction w.r.t[35] | | 37.03 | 50 | 37.03 | 9.72 | 33.33 |
| Existing[36] | 3 majority gates and one inverter | 34 | 33534 | 11016 | 32.85 | 4 |
| Percentage reduction w.r.t[36] | | 50 | 65.22 | 50 | 14.37 | 50 |
| Existing[37] | 3 majority gates and 3 inverters | 34 | 33696 | 11016 | 32.69 | 4 |
| Percentage reduction w.r.t[37] | | 50 | 64.90 | 50 | 14.53 | 50 |
| Existing[38] | 3 majority gates and one inverter | 26 | 15552 | 8424 | 54.16 | 2 |
| Percentage reduction w.r.t[38] | | 34.61 | 25 | 34.61 | -6.96 | 0 |
| Existing[39] | 3 majority gates and one inverter | 25 | 21600 | 10000 | 46.29 | 3 |
| Percentage reduction w.r.t[39] | | 32 | 46 | 44.92 | 0.93 | 33.33 |
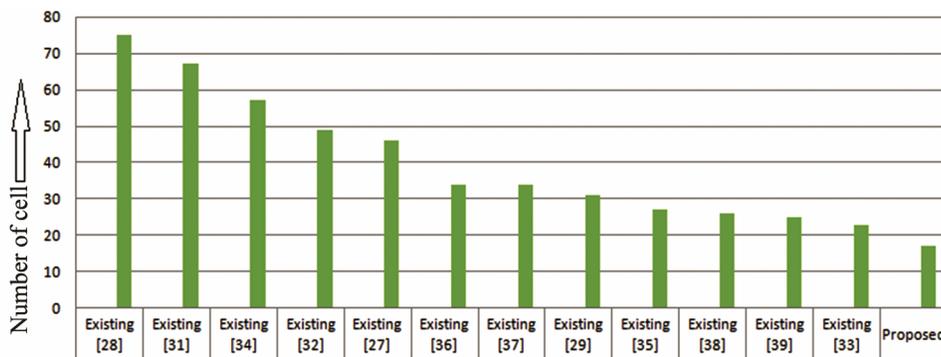


Fig. 14 – Number of cell of proposed 2:1 MUX and previous design

| Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [39] | Existing [35] | Existing [38] | Existing [33] | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24300 | 21708 | 18468 | 15876 | 14904 | 11016 | 11016 | 10044 | 10000 | 8748 | 8424 | 7452 | 5508 |

Fig. 15 – Cell area of proposed 2:1 MUX and previous design



| Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [39] | Existing [33] | Existing [38] | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 99792 | 81648 | 72900 | 46332 | 46332 | 33534 | 33696 | 37908 | 23328 | 21600 | 18144 | 15552 | 11664 |

Fig. 16 – Total area of proposed 2:1 MUX and previous design



| Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24.35 | 26.58 | 25.33 | 34.26 | 32.16 | 32.85 | 32.69 | 26.5 | 37.5 | 54.16 | 46.29 | 41.07 | 47.22 |

Fig. 17 – Area usage of proposed 2:1 MUX and previous design



| Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] | Proposed |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 4 | 4 | 2 | 4 | 4 | 4 | 4 | 3 | 2 | 3 | 3 | 2 |

Fig. 18 – No of clock zones of proposed 2:1 MUX and previous design
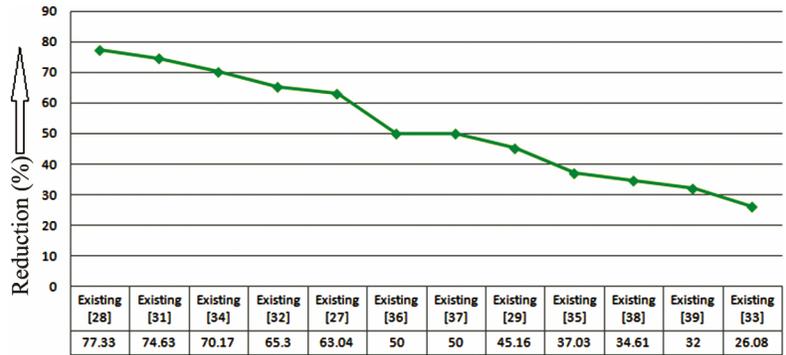
Fig. 19 – Percentage reduction of cell of proposed 2:1 MUX than previous design

| | Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 77.33 | 74.63 | 70.17 | 65.3 | 63.04 | 50 | 50 | 45.16 | 37.03 | 34.61 | 32 | 26.08 |
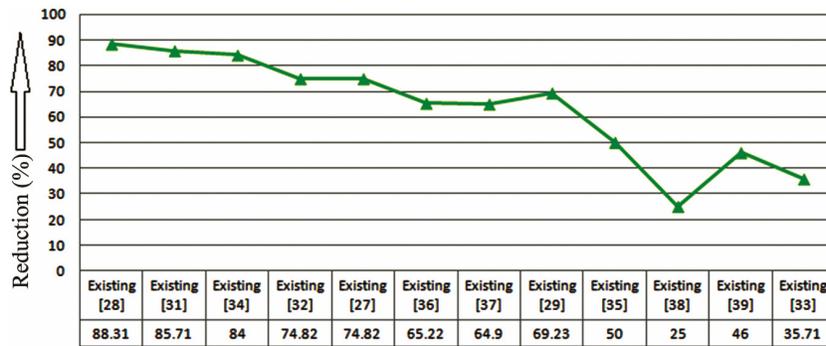


Fig. 20 – Percentage reduction of total area of proposed 2:1 MUX than previous design

| | Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 88.31 | 85.71 | 84 | 74.82 | 74.82 | 65.22 | 64.9 | 69.23 | 50 | 25 | 46 | 35.71 |
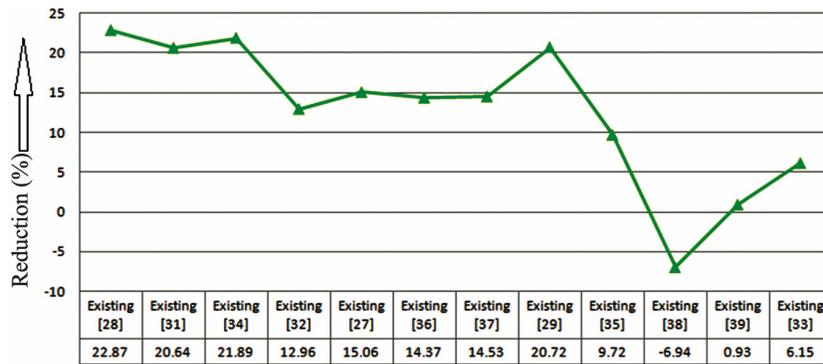


Fig. 21 – Percentage reduction of area usage of proposed 2:1 MUX than previous design

| | Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 22.87 | 20.64 | 21.89 | 12.96 | 15.06 | 14.37 | 14.53 | 20.72 | 9.72 | -6.94 | 0.93 | 6.15 |
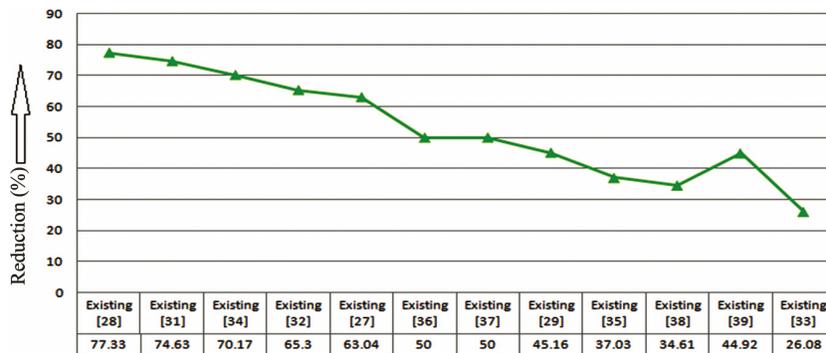


Fig. 22 – Percentage reduction of cell area of proposed 2:1 MUX than previous design

| | Existing [28] | Existing [31] | Existing [34] | Existing [32] | Existing [27] | Existing [36] | Existing [37] | Existing [29] | Existing [35] | Existing [38] | Existing [39] | Existing [33] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 77.33 | 74.63 | 70.17 | 65.3 | 63.04 | 50 | 50 | 45.16 | 37.03 | 34.61 | 44.92 | 26.08 |
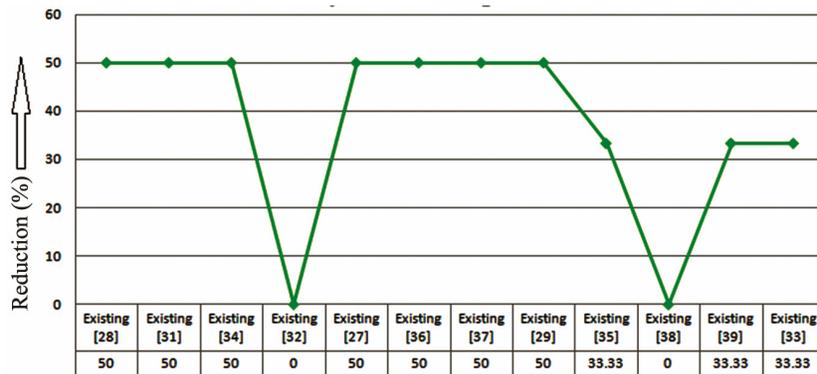
Fig. 23 – Percentage reduction of clock zones of proposed MUX than previous design

## 4 Conclusions

The correctness of the proposed circuit is verified with theoretical values. Proposed 2:1 MUX circuit required 17 cells and 11664 nm² areas but usage area is only 47.22%. Comparison with previously designed MUX shows that the proposed circuit design is denser and faster in terms of area consumed by the circuit and clocking zones, respectively. The circuits can be used to build advanced complex multiplexers like 4:1 MUX, 8:1 MUX etc. in future at nanoscale. The circuit can also play a major role in the field of digital nanocommunication for signals encoding in near future.

## Acknowledgement

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