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# Capacitor voltage balancing in *dc* link five-level full-bridge diode-clamped multilevel inverter

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The voltage balancing of dc capacitors is a great problem of all multilevel with several dc link. The chopper circuit in a five-level full-bridge diode-clamped multilevel inverter to overcome the unbalance charging of capacitor voltage has been studied in the present paper. The proposed chopper circuit requires additional inductors and control scheme, is very simple to implement and its different operation modes are described in the present paper. Simulation and experimental results are presented to verify the proposed chopper circuit for dc capacitor voltage balancing in the five-level full-bridge diode-clamped multilevel inverter and show that it can reduce a total harmonic distortion of output voltage and current.

Keywords: Capacitor voltage balancing, Chopper, Diode-clamped multilevel inverter

#### **1** Introduction

Multilevel inverters are used in high power and high voltage applications. Their output voltage produces a staircase output waveform which looks like a sinusoidal waveform. The output voltage having less number of harmonics as compared to the conventional bipolar inverter output voltage. If the number of levels of the multilevel inverter is increased to an infinite level, consequently the harmonics reduced to the output voltage value to zero. Multilevel inverters are mainly classified as diodeclamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and cascaded multilevel inverter (CMLI) with separate dc source. The advantages of DCMLI are; dc capacitors can be easily pre-charged, control of switched is very simple<sup>1</sup>, protection circuit is less complex than other multilevel inverter<sup>2,3</sup>. A DCMLI provides multiple voltage levels through connection of the phases to series bank of capacitors. The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages. Problem of all multilevel inverter topology with several dc links is voltage balancing of dc capacitors. For operation of DCMLI under different conditions, the voltage divisions on the capacitors are unequal, consequently quality of multilevel inverter is reduced. The methods used to overcome the unbalanced charging of capacitor voltage are; changing the switching pattern<sup>4,5</sup>, installation of capacitor voltage balancing circuits on the dc side of the multilevel inverter<sup>1,6</sup>. For multilevel inverters with the space vector pulse width modulation (SVPWM) method proposed<sup>7,8</sup>, can be selected to balance dc link capacitor voltages without some auxiliary circuits; however, the SVPWM method work only in a low modulation index range and output voltage quality is decreased but the control algorithm complexity of the SVPWM method is increased<sup>9</sup>. To overcome the unbalance charging of capacitors voltage; the first solution is preferable in term of reducing the complexity of system, cost and additional circuits that are used to overcome the unbalance charging of capacitor voltage, are conventional choppers<sup>1</sup>. Output ripple, size and weight of conventional choppers depend on increasing switching frequency but the consequences are high stress on switches, high switching losses and high electromagnetic interference<sup>4,10</sup>.

The chopper circuit used to overcome the unbalance charging of capacitor voltage of a single phase 5-level full-bridge diode-clamped multilevel inverter without increasing the circuit size and weight, has been studied in the present paper. Simulation and experimental results are presented to verify and validate features of proposed topology.

### 2 Diode-Clamped Multilevel Inverter

An m-level diode-clamped inverter typically consists of  $m^{-1}$  capacitors on the *dc* bus voltage and produces m levels of the phase voltage. Figure 1



Fig. 1 — Single-phase 5-level full-bridge DCMLI

| Table 1— Switching scheme of 5-level full-bridge DCMLI |       |       |       |       |          |                        |                        |          |
|--|-------|-------|-------|-------|----------|------------------------|------------------------|----------|
| $V_{ab}$   | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_{11}$ | <i>S</i> <sub>22</sub> | <i>S</i> <sub>33</sub> | $S_{44}$ |
| $V_{dc}$   | 1     | 1     | 1     | 1     | 0        | 0                      | 0                      | 0        |
| $V_{dc/2}$   | 0     | 1     | 1     | 1     | 1        | 0                      | 0                      | 0        |
| 0  | 0     | 0     | 1     | 1     | 1        | 1                      | 0                      | 0        |
| $-V_{dc/2}$  | 0     | 0     | 0     | 1     | 1        | 1                      | 1                      | 0        |
| $-V_{dc}$  | 0     | 0     | 0     | 0     | 1        | 1                      | 1                      | 1        |

shows a single-phase 5-level full-bridge diodeclamped multilevel inverter in which the dc bus voltage consists of four capacitors; C<sub>1</sub>, C<sub>2</sub>, C<sub>3</sub>, and C<sub>4</sub>. For a dc bus voltage  $V_{dc}$ , the voltage across each capacitor is  $V_{dc}/4$  and each device voltage stress will be limited to a capacitor voltage level,  $V_{dc}/4$ , through clamping diodes. Table 1 presents switching scheme of the 5-level full-bridge DCMLI that state 1 means switch turns on and state 0 switch turns off.

There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. Techniques<sup>11</sup> can be efficiently applied for DCMLI known as PD, POD and APOD. Phase Opposition Disposition (POD) techniques are used as shown in Fig. 2 that all carrier signals above the zero axis have same frequency, same amplitude and in phase with each other. But below the zero axis, all the carrier signals have phase shifted 180 degree as compared to the above zero axis carrier waveform and have same frequency, same



Fig. 2 - POD PWM of a 5-level multilevel inverter



Fig. 3 — Relationship between the sinusoidal reference signal and the triangular signal

amplitude in phase with each other<sup>12</sup>. In multilevel inverters, the amplitude modulation index  $(m_a)$  is the ratio of reference amplitude  $(A_m)$  to carrier amplitude  $(A_c)$ , can be written as in Eq. (1). The frequency ratio  $(m_f)$  is ratio of carrier frequency  $(f_c)$  to reference frequency  $(f_m)$ , can be written as in Eq. (2).

$$m_a = A_m / (m-1)A_c \qquad \dots (1)$$

$$m_f = f_c / f_m \qquad \dots (2)$$

Figure 3 shows the relationship between the sinusoidal reference signal and the triangular signal used to create the PWM signal; the output of the PWM signal is either 1 when  $V_{ctrl} > V_{tri}$ , or 0 when  $V_{ctrl} < V_{tri}$  and the PWM signal width, can be written as in Eq. (3).

$$T_{\rm PWM} = A_{\rm ctrl} \cdot T_{\rm tri} \quad , 0 \le A_{\rm ctrl} \le 1 \qquad \dots (3)$$

where  $T_{\text{PWM}}$  is width of the PWM signal,  $A_{\text{ctrl}}$  the height of the control signal,  $T_{\text{tri}}$  the period of the triangular signal,  $V_{\text{ctrl}}$  the output voltage of the control signal and  $V_{\text{tri}}$  is output voltage of the triangular signal.



Fig. 4 —Signals for controlling a DCMLI

| Table 2 — Control signals of a 5-level DCMLI |   |  |  |  |  |
|--|---|--|--|--|--|
| Switches                                     | Digital process   |  |  |  |  |
| $S_1$  | $\mathbf{PWM} \cdot G_1 \cdot G_2$  |  |  |  |  |
| $S_2$  | $(\text{PWM} \cdot G_1 \cdot \overline{G_2}) + (G_1 \cdot G_2)$                         |  |  |  |  |
| $S_3$  | $(\overline{\text{PWM}} \cdot \overline{G_1} \cdot \overline{G_2}) + (G_1)$             |  |  |  |  |
| $S_4$  | $(\overline{\mathrm{PWM}} \cdot \overline{G_1} \cdot G_2) + (\overline{G_1} \cdot G_2)$ |  |  |  |  |
| $S_{11}$                                     | $\overline{S_1}$  |  |  |  |  |
| $S_{22}$                                     | $\overline{S_2}$  |  |  |  |  |
| S <sub>33</sub>                              | $\overline{S_3}$  |  |  |  |  |
| $S_{44}$                                     | $\overline{S_4}$  |  |  |  |  |

Figure 4 shows output waveform of a 5-level fullbridge DCMLI, is generated from the control signals which are PWM,  $G_1$ , and  $G_2$  signals as shown in Fig. 4. Table 2 presents the modulated signal applied from Eqs (4) and (5).

$$T_{\rm PWM} = m_a \cdot T_{\rm tri} \cdot \sin(\omega t), \begin{cases} 0 \le \omega t < \frac{\pi}{6} \\ \frac{5\pi}{6} \le \omega t < \pi \end{cases}$$
(4)

$$T_{\text{PWM}} = m_a \cdot T_{\text{tri}} \cdot \left(2\sin\left(\omega t\right) - 1\right) \quad , \frac{\pi}{6} \le \omega t \le \frac{5\pi}{6} \qquad \dots (5)$$

Simulation results of control signals of the 5-level DCMLI based on PSCAD/EMTDC with  $m_a = 0.9$ ,  $f_c = 3600$  Hz, and  $f_m = 50$  Hz; Fig. 5(a) shows main control signals based on Eqs(4) and (5) and Fig. 5(b) shows switch control signals in Table 2.



(a) Main control signals based on Eqs (4) and (5)



(b) Switch control signals based on digital process

Fig. 5 — Control signals of the 5-level DCMLI

### **3 Proposed Chopper Circuit**

Proposed chopper circuit is shown in Fig. 6(a) that its objective is to overcome the unbalance charging of capacitor voltage. The resistances  $RL_1$  and  $RL_2$  in Fig. 6(a) represent the winding resistances of the corresponding inductors. The capacitor voltages are controlled within a band by transferring the extra energy from the overcharged capacitor to an inductor and then transferring it back from the inductor to the undercharged capacitor. This chopper consists of two parts. In the upper part;  $L_1$  is used to exchange the energy between  $C_1$  and  $C_2$  using  $St_1$ ,  $St_2$  and in the lower part,  $L_2$  exchanges the energy between  $C_3$  and  $C_4$  using  $St_3$ ,  $St_4$ . Fig. 6(b-f) shows its operation in different modes that voltage and current waveforms in different operation modes as shown in Fig. 7.



(a) The proposed chopper circuit (b)  $S_{t1}$  and  $S_{t4}$  turn-on



(c)  $S_{t1}$  turns-on (d)  $S_{t2}$  turns-on



(e)  $S_{t2}$  and  $S_{t3}$  turn-on (f)  $S_{t4}$  turns-on

Fig. 6 — Different operation modes of proposed chopper

In the proposed chopper, the capacitors are charged to their order, according to the sequences of switching states which are shown in Fig. 7 consequently, the charging process is very fast. The block diagram of proposed control method is shown in Fig. 8 that is very simple to implement the presented control. In Fig. 8; the switching frequency is 3600 Hz, the  $S_{t1}$  is controlled by PWM signal with duty cycle 20%, the  $S_{t2}$  by PWM signal with duty cycle 40%, the  $S_{t3}$  by PWM signal with duty cycle 10%, and the  $S_{t4}$  by PWM signal with duty cycle 50%.



Fig. 7 — Voltage and current waveforms in different modes of proposed chopper circuit



Fig. 8 — Control block diagram of balancing capacitor voltage of the five-level full-bridge DCMLI

To validate the proposed chopper, the five-level full-bridge diode-clamped multilevel inverter supplying an R-L load (R = 30  $\Omega$ , L = 50 mH) with 310 V *dc* link voltage is simulated by PSCAD/EMTDC. Simulation results' voltage value of 4 capacitor is  $V_{dc}/4$  (310/4 = 77.5 V) are shown in Fig. 9(a), and output voltage and current waveforms are shown in Fig. 9(b).

#### **4 Experimental Results**

Figures 10 and 11 show the topology and the prototype of five-level full-bridge diode-clamped multilevel inverter rated 2.2 kW with capacitor voltage balancing used IGBT modules (CM75DU-12H) as power electronic switches which are controlled by



(a) Capacitor voltage



(b) Output voltage and current waveforms

Fig. 9 — Simulation results based on PSCAD/EMTDC



Fig. 10 — Topology of the five-level full-bridge DCMLI



Fig. 11 — Prototype of the five-level full-bridge DCMLI



Fig. 12 — Control signals by DSP controller

TMS320F28027 DSP controller and used RURG8060 Ultrafast Diode to be diode-clamped. The chopper inductor are taken as  $L_1 = L_2 = 25 \ \mu H$ , capacitors are taken as  $C_1 = C_2 = C_3 = C_4 = 3300 \ \mu F$ , and *dc*-link voltage is 310 V.

Figure 12 shows four control signals which consist of  $G_1$ ,  $G_2$ , PWM and PWM based on phase opposition disposition techniques created by TMS320F28027 DSP controller with  $m_a = 0.9$ ,  $f_c = 3600$  Hz, and  $f_m = 50$  Hz. Figure 13 shows control signals of the 5-level DCMLI which consist of  $s_1$ ,  $s_2$ ,  $s_3$  and  $s_4$  based on Table 2.



Fig. 13 — Control signal of 5-level DCMLI



Fig. 14 — Output voltage waveform of the 5-level full-bridge DCMLI without voltage balancing circuit



Fig. 15 — Output voltage THD of the 5-level full-bridge DCMLI without voltage balancing circuit is 22.4%



Fig. 16 — Output current waveform of the 5-level full-bridge DCMLI without voltage balancing circuit



Fig. 17 — Output current of the 5-level full-bridge DCMLI without voltage balancing circuit is 4.4%

Experimental result of a five-level full-bridge diode-clamped multilevel inverter without voltage balancing circuit with R-L load ( $R = 30 \Omega$ , L = 50 mH); output voltage waveform is shown in Fig. 14, output voltage THD is 22.4% as shown in Fig. 15, output current waveform is shown in Fig. 16, and output current THD is 4.4% is shown in Fig. 17.

For experiment to validate the proposed chopper in the five-level full-bridge diode-clamped multilevel inverter supplying an R-L load ( $R = 30 \Omega$ , L = 50 mH) with 310V *dc* link voltage. Experimental results; *dc* link voltage of  $C_1$  to  $C_4$  is  $V_{dc}/4$  (310/4 = 77.5 V) as shown in Fig. 18, output voltage and current



Fig. 18 — DC link capacitor voltage of  $C_1$  to  $C_4$  is 77.5V



Fig. 19 — Output voltage and current waveforms of the 5-level full-bridge DCMLI with voltage balancing circuit



Fig. 20 — Output voltage THD of the 5-level full-bridge DCMLI with voltage balancing circuit is 18%



Fig. 21 — Output current of the 5-level full-bridge DCMLI with voltage balancing circuit is 3.7%

waveforms are shown in Fig. 19, output voltage THD is 18% as shown in Fig. 20, and output current THD is 3.7% as shown in Fig. 21.

## **5** Conclusions

Chopper circuit for dc capacitor voltage balancing in five-level full-bridge diode-clamped multilevel inverter has been proposed in the present paper. It requires additional inductors and control scheme is very simple to implement. The different operation described according to modes are Fig. 7. Experimental results of the prototype inverter with R-L load ( $R = 30 \Omega$ , L = 50 mH) show that the proposed chopper circuit can overcome the unbalance charging of capacitor voltage, the percentage of voltage THD and current THD are less than versus the inverter without proposed chopper circuit.

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