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A 128Kb RAM Design with Capacitor-Based Offset Compensation and Double-Diode based Read Assist Circuits at Low V_{DD}

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Low power static random access memory (SRAM) takes significant portion of area on chip in all modern SOCs and emerging Computing-in-memory applications for edge devices in IoT. This work proposes novel readability assist with the double-diode based word line under drive (WLUD) has been effective improving the read-static noise-margin (RSNM) by 26–46%and proposed a capacitor based current controlled sense amplifier offset compensation scheme. This scheme achieves 4X reduction in standard deviation of offset voltage over conventional sense amplifier design with 1.1% and 2.9% of area, power overheads respectively with 90 nm CMOS technology at 0.5–1.0 V supply voltages.

Keywords: Current-controlled sense amplifier (CCSA), Offset cancellation, RSNM, SRAM, WLUD

Introduction

In order to handle the computations and operations associated with the development of complex convolution neural network systems, it also requires possessing an in-memory computation capability.[1] Low power static random access memories (SRAM) are popular embedded memories due to their low static power consumption and low latency.[2,3] With supply voltage (V_{DD}) scaling, SRAM designs suffer from uncertainty of read operation, offset voltage, large leakage currents and degraded RSNM read-static noise-margin (RSNM). Bias Temperature Instability (BTI) is also a dominant issue in the transistors and affects the SNM of SRAM cells.[4] For reduction of BTI, a three-step technique is proposed.[5]

Experimental Details

Conventional Read Assist (RA) and Sense Amplifier (SA) circuits

To improve the RSNM, in memories also require read-assist (RA) circuits. Recent RA circuits were implemented using word line under drive (WLUD) scheme to improve RSNM as it would help in reducing energy consumption. WL voltage is controlled using row-based RA technique of WLUD in which pass gate strength can be lowered.[6–8] Consequently, it improves the read stability, degrading read performance, and write-ability. To improve write-ability, it is necessary to degrade the strength ratio of pull up (PU) and pull down (PD). It can be achieved by using charge sharing transient voltage collapsing (C*V*DD, CELL)[9] and a charge redistribution transient voltage collapsing write assist (CR-TVC-WA) was proposed.[10] In this work, a diode based WLUD and double-diode based WLUD has been proposed and it provides better RSNM and improves the read stability of memory design, but degrades the write ability. For further improving the write ability, existing CR-TVC-WA technique is used in our design.[10]

With CMOS technology scaling, another major design issue in SRAM is increase in threshold mismatches and variations which affects the corresponding off-set voltages (OSV).[12] The OSV issues by incorporating compensation and calibration methods. However, according to the calibration techniques demonstrated by Singh & Bhat (2004)[(11)], observing delay in the rise-time of the SA is one such technique. Several other calibration methods are suggested and investigated. The body-biasing (BB) is also explored for the similar purpose.[13–16] Singh & Bhat (2018)[(12)] reported the simple differential and

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common mode boosting techniques that can provide 23% improvement in the off-set.

The compensation-based technique is demonstrated and evaluated[13] with capacitors. Similarly, in the proposed method, several capacitors are employed. These capacitors are used to preserve any mis-match voltage from the corresponding transistor at the input. A capacitor-based SA technique which is considered as an enhanced version is mentioned.[17] The enhancement involves in employing differential sensing along with current mode. The capacitor employed is responsible for the offset reduction. Similarly, our proposed capacitor based current controlled SA[17] technique can be considered as an extension to analysis of area and power.

Results and Discussion

Design and Analysis of Proposed Sense Amplifier

The SA is known to possess very high speed of operation. Especially, the latch type SA (LSA) consumes less power and also has quite non-complex circuit for implementation. In this work, an NMOS type input LSA based design is presented. It is conveniently suitable to handle extremely low voltages. The corresponding circuit is as shown in Fig. 1(a). Before the sense amplifier starts operation, the signal SAE is low and at this condition, transistor N5 is turned OFF, and P3 and P4 are ON, so node Q and QB are high and close to V_{DD}. In sensing period, SAE turns high, then N5 turns ON, sense amplifier starts sensing. At this moment, as can be seen, only the mismatch between input NMOS pairs (N3-N4) and sensing devices (N1-N2) contributes to SA's offset. The mismatch between P1 and P2 can be ignored.

The sense-amplifier offset is mostly affected by the threshold voltage mismatches between the NMOS devices of the cross coupled inverters. The proposed circuit uses NMOS capacitors. These capacitors referred as C0 as well as C1. These are responsible for storing the threshold voltages. This is obtained from

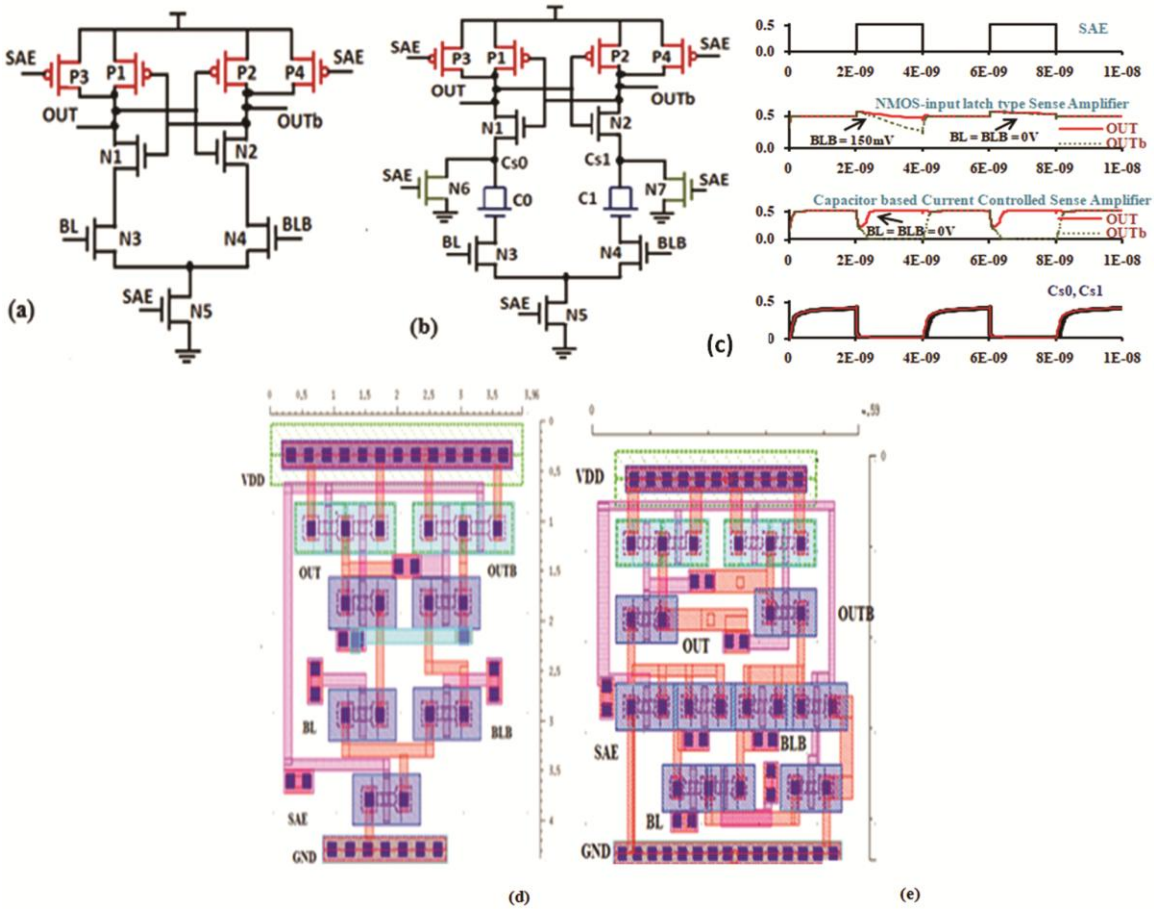

Fig. 1 — (a) NMOS – i/p LSA[16], (b) Capacitor- based CCSA[17], (c) Transient response of Proposed Sense Amplifier; Layout of (d) Conventional SA, (e) Capacitor based CCSA

the critical input transistors. This knowledge of the voltage is later used in the process of compensation. The compensation is carried out with reference to the threshold mismatches.[17]

The offset compensated SA model is presented in Fig. 1(b). The elements N6 as well as N7 are transistors. These are responsible for providing desired threshold balancing of C0 and C1 for compensating the off-set during the sensing process. The SA can have either of the set or reset states. During the state of "reset" the SAE will have 0. At his state the SA out-put develop VDD across their nodes. This also results in the terminals which are represented by C_{s0} and C_{s1} to pre-charge to VDD − VT, N1 and VDD − VT, N2 respectively. Here VT, N1 as well as VT, N2 are referred as threshold voltages. These two appear at N1 and N2. The state "SAE=1" is explained as the progress of read operation. While the read phase is in progress, along with the read operation, the corresponding compensation of the off-set also initiates. This consistently develops differential across the BL and BLBs. This is obvious as the WL is asserted. The C0 as well as C1 pulls Cs0 along with Cs1 nodes to the state of "LOW". Now, the corresponding N1 along with N2 transistors are supposed to be turned ON. This considerably results in the amplification of the input differential. The following plot in Fig.1(c) demonstrates the same in which the trend of the transients can be witnessed.

As mentioned previously, the proposed methodology[13] uses two unique signals. These two are used to compensate the respective off-sets. In this work, a conventional design-based approach is presented with only one signal. As a result, it can considerably avoid the need for another additional signal for SA implementation.

The layouts in 90 nm CMOS of conventional SA and proposed capacitor based current controlled SA designs are shown in Fig.1 d & e. The area of each capacitor based current controlled SA is 4.59 µm × 4.46 µm, the area of SA without capacitors is 3.96 µm × 4.41 µm as shown in Fig. 1 (d) & (e) and the SRAM memory cell area is 3.3 µm × 3.94 µm. The capacitors are added to the sense amplifier to offset compensation result in only an additional 1.1% of area overhead for a 64 Kbit memory macro. Additionally, the memory array consumed the 2.9% of power due to capacitor-based SA with compared to conventional SA.

Simulations of the Proposed SA

Under normal conditions, the offsets are computed using the Monte-Carlo methods. These are clearly mentioned in SA as given in Fig.2 a & b. It is also termed as input referred offset (IRO). It also can be inferred that this IRO is improved when compared

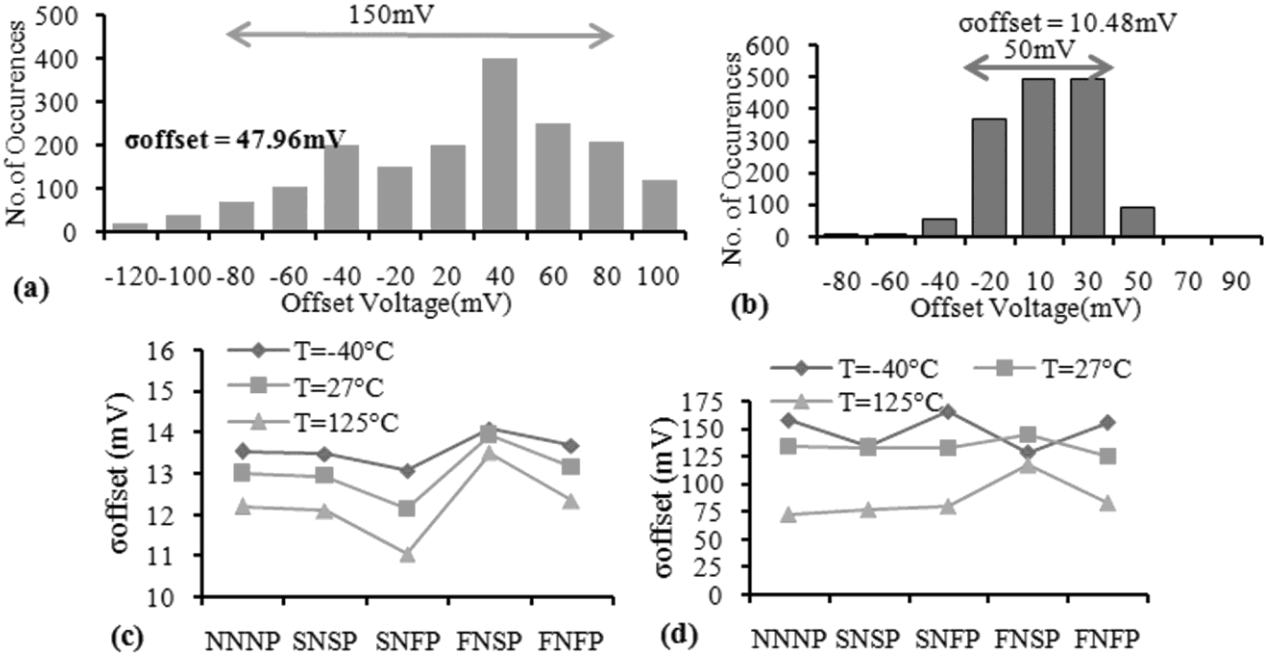

Fig. 2 — Histograms of 1000 MC simulations: (a) before offset compensation, (b) after offset compensation; Standard deviation of offset voltage with process corners with temperature variation (c) Proposed SA, (d) Conventional SA

with the conventional type of SA. The magnitude of this enhancement in the IRO is almost more than 50% with respect to that of the conventional model.

The σ of off-set voltage with different process corners and temperature variations are shown in Fig. 2 c & d. The sense amplifiers offset voltage is calculated based on Monte Carlo simulations with mismatch NMOS transistors of cross coupled inverters and 3σ random variation. At T=125°C, provides the lower offset voltage compared to various temperatures. Especially SF corner provides the lower offset voltage in proposed SA. the efficiency of the proposed capacitor-based SA are further summarized in Table 1.

Design and Analysis of Proposed Read Assist Circuit

Word line under drive is required to enhance the RSNM as well as the Read stableness in the design. Considering the PMOS and NMOS transistor threshold voltages (V_{th}) at various process corners such as Slow(S), Fast (F) and Normal (N). A dual-tracking WLUD[8] provides the efficient control over the stray supply node due to WL driver. The dual-tracking WLUD circuit consists of one PMOS device, P2 and NMOS device, N2 which tracks the WL driver pull-up and cell access through NMOS. The gate of PMOS P2 can also be connected to the GND.

The WL rise time is increasing without WLUD in comparison with dual tracking WLUD. This dual tracking WLUD degrades the amounts of WL driver voltage compared to proposed WLUDs. In this paper a diode based WLUD and Double-diode based WLUD are proposed as shown in Fig 3 (a) & (b). The proposed diode based WLUD circuit comprises of dual tracking WLUD where the NMOS transistor drops the voltage to ground. Hence WL voltage is

Table 1 — Performance comparisons of proposed SA design

Parameters	Comparison of proposed method with existing literature				
	[13]	[15]	[14]	[16]	Proposed method
Supply (V)	0.9	0.5–1.2	0.4–1.2	1.8	0.5–1.0
Technology (nm)	28	130	65	180	90
Off-set Scheme	Compensation	Calibration	Calibration	Calibration	Compensation
Sensing Mode	Voltage mode	Current mode	Current mode	Current mode	Current mode
Off-set reduction	1.5X	4.5X	2X	1.91X	4X
Area Over-head	3.2%	6.5%	3.5%	7.5%	1.1%
Power Over-head	—	1.6%	1%	—	2.9%

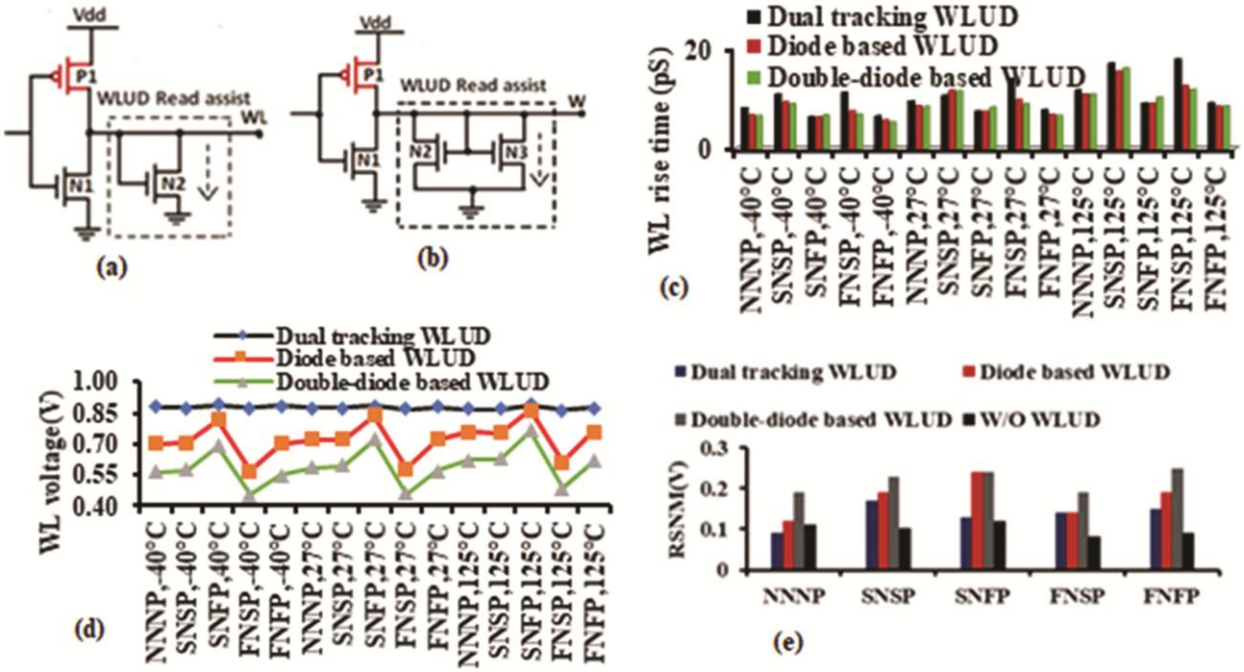

Fig. 3 — Proposed WLUDs across various process corners with temperatures at V_{DD} = 1.0V: (a) Diode based; (b) Double-Diode based; (c) WL rise time; (d) WL voltage; (e) RSNM of WLUDs

reduced. The technique appears to be very simplified in terms of providing WL voltage similar to dual tracking WLUD at process corner SF. At the remaining process corners provides the degradation of WL voltage as shown in Fig. 3 (d).

Another proposed double-diode based WLUD consists of two NMOS transistors. It discharges the voltage unlike in dual tracking WLUD and diode based WLUD. The NMOS transistor gate terminal is connected to WL driver. When WL drive is selected, it degrades the WL voltage. However, due to the presence of N2 and N3 are connected to ground path, it lowers WL level and degrades WL rise time. At process corner SF provides less amount degradation of WL voltage compare to remain process corners as shown in Fig. 3 (d).

The proposed double-diode based WLUD provides suppressed WL voltage. Also, it results in good rise-time and better process corners with temperature variation at −40.0°C, 27°C and 125°C. The WL rise time of the proposed WLUDs across various process corners and temperatures at V_{DD}= 1.0V are compared in Fig. 3(c). The proposed scheme provides the lowest WL rise time at FNFP (Fast NMOS Fast PMOS) corner and the highest WL rise time at SNSP (Slow NMOS Slow PMOS). The comparison of RSNM with proposed WLUDs at different process corners are shown in Fig. 3(e). When device is treated under the process corners are FNSP and SNFP, at V_{DD} = 1.0V RSNM has an improvement of 45.8% and 26.3% respectively.

The WL voltage level of the proposed WLUDs and dual tracking WLUD scheme across various process corners at V_{DD} are compared in Fig.3 (d). It can be observed that there is considerable effect of the WL-voltage on other parameters. Once this WL-voltage goes lower, the corresponding effect on the channel is evident. This significantly enhances the resistance of N2 and N3. On the other hand, it is also possible to witness the diminishing current along N2/N3 voltage level at SNFP (Slow NMOS Fast PMOS) corner (Where RSNM is best) as shown in Fig. 3 (d). In this technique, the least WL voltage level at FNSP (Fast NMOS Slow PMOS) corner is possible along with enhanced respective WL.

Finally, 128 kb SRAM array has been designed with the proposed read assist circuit and sense amplifier circuits. Then, the 128kb SRAM array is tiled with 256 × 256 macro bit cell array with 2b write masking, WL and column decoder-array, sense amplifier, and write/read buffers. In this array, the proposed capacitor based current controlled SA and Double-diode based WLUD are used.

Conclusions

This work demonstrates WLUD read assist circuit and capacitor based current controlled sense amplifier for a 128Kb 90 nm CMOS 6T SRAM array. The evaluation of WLUD read assist circuits considering various process corners and temperature variations is done. The double-diode based WLUD read assist provides better RSNM compared to the diode based WLUD and dual tracking WLUDs. At V_{DD} = 1.0 V, the RSNM improvement has been 45.8% for FNSP and 26.3% for SNFP process corners, respectively. The work further demonstrates a sense amplifier offset compensation with capacitor based current controlled scheme with 0.5–1.0 V operation. The proposed offset compensation technique achieved ~ 4X off-set improvement with an area overhead of 1.1% and power overhead of 2.9%, respectively. Finally, the simulations reveal that read assist can reduce the rise time and has improved the read V_{MIN} of fast-N fast-P corner at −40.0°C, 27.0°C and 125.0°C respectively.

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